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(54) DIGITAL SIGNAL REPRODUCTION DEVICE

(57)Abstract:
PURPOSE: To reduce the circuit scale of a special reproduction circuit by a digital VTR adopting an encoding system represented by MPEG 2.
CONSTITUTION: A digital VTR which transparently records data of an inputted MPEG 2 packet and reproduces recorded data is provided with a data separation means 24 separating special reproduction data constituted by using data of an intraframe and a still picture slice data generation means 30 generating slice data where moving vector is '0' and a prediction error is '0' by all macro blocks in a slice. The still picture slice generation means 30 is controlled in such a way that the outputs of the still picture slice generation means 30 are outputted by the prescribed number of fames after special reproduction data for 0111 frame or one field separated from a data storage means are outputted.

CLAIMS

[Claim(s)]
[Claim 1]the inside of a frame characterized by comprising the following inputted in the state of a packetor the field -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outDigital signal playback equipment in which data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedand data for special reproduction generated [above-mentioned] reproduces a recording medium currently recorded on a position.

A data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproduction.
A data storage means which memorizes the separated above-mentioned data for special reproduction.
All the macro blocks in a slice have a still picture slice data generating means in which a motion vector generates slice data whose prediction error is 0 in 0A data control means which controls the above-mentioned still picture slice generating means so that predetermined carries out the frame number partial output of the output of the above-mentioned still picture slice generating means after outputting one frame separated from said data storage meansor the above-mentioned data for special reproduction for the 1 field.

[Claim 2]the inside of a frame characterized by comprising the following inputted in the state of a packetor the field -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outDigital signal playback equipment in which data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedand data for special reproduction generated [above-mentioned] reproduces a recording medium currently recorded on a position.
A data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproduction.
A data storage means which memorizes the separated above-mentioned data for special reproduction.
All the macro blocks in a slice have a still picture slice data generating means in which a motion vector generates slice data whose prediction error is 0 in 0The above-mentioned data for special reproduction separated from regenerative data reproduced intermittently by the above-mentioned data separation means 1 or plural slicesWhile considering it as a transport packet for one **** for an output of a still picture slice data generating meansthe above-mentioned transport packet And the fieldOr a packet creating means which constitutes a packet so that data for special reproduction which considered it as a packet in inter-frame-prediction modeand was reproduced by the above-mentioned intermittent target may be made into the compulsory intra-frame mode and may be transmitted.

[Claim 3]The digital signal playback equipment according to claim 1 performing the above-mentioned data switching control means at the time of still playback so that an output in the above-mentioned still picture packet creating means may always be chosen after an end of a final data output of the above-mentioned frame or a frame reproduced at the time of ordinary reproduction.
[Claim 4]Until a servo system locks and intra-frame data for [above-mentioned] special reproduction is reproduced from the above-mentioned fast reproduction area at the time of mode transition to fast reproductionThe digital signal playback

equipment according to claim 1 characterized by performing the above-mentioned data switching control means so that an output of the above-mentioned still picture packet creating means may be chosen.
[Claim 5]The digital signal playback equipment according to claim 2 using the above-mentioned control system at least at the time of special reproduction of an opposite direction.
[Claim 6]the inside of a frame or the field inputted in the state of a packet -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outData for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn digital signal playback equipment in which data for special reproduction generated [above-mentioned] reproduces a recording medium currently recorded on a positionWhen a data separation means which separates the above-mentioned data for special reproduction from a regenerative signaland data outputted from a digital signal recording and reproducing device are decoded and reproduced image data is restoredWhen it has a specific area fixed packet creating means which generates a packet for standing a signal of specific area on a screen still and a reproduced image is constituted using data reproduced intermittently at the time of special reproductionan output of the above-mentioned specific packet fixing meansDigital signal playback equipment switching the above-mentioned regenerative data and controlling to divide the above-mentioned data for special reproduction of one frame into a multiple frameand to transmit it.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention A compact disc player (it is hereafter described as CD.)a digital audio tape recorder. (it is hereafter described as DAT.) -- a digital video signal recording and reproducing device. (it is hereafter described as a digital video tape recorder.) -- or it is related especially with the interface control at the time of special reproduction about digital signal playback equipmentsuch as a digital video tape recorder which records the bit stream of the digital video signal and digital audio signals which are represented by MPEG 2 etc.
[0002]
[Description of the Prior Art]Drawing 29 is a track pattern figure of a common home digital video tape recorder. In the figurethe slanting track is constituted by magnetic tape and one track is divided into two areathe image area which records a digital video signaland the audio area which records digital audio signals.
[0003]There are two methods in recording an image and an audio signal on such a home digital video tape recorder. One is what is called a baseband recording

method recorded by considering an analog video signal and an audio signal as an input using the highly efficient coding equipment of an image or an audio. Another is what is called a transparent recording method that records the bit stream transmitted digitally.

[0004]In order to record the ATV (Advanced Television) signal currently deliberated in the United States of Americathe latter transparent recording method is suitable. The reason is the signal with which digital compression of the ATV signal was already carried out.

It is that highly efficient coding equipment and a decryption machine are unnecessarythat there is no degradation of image quality since it records as it isetc.

On the other handas demeritit is the image quality at the time of fast reproductionand a still and which slow special reproduction. A picture is hardly unreproducible at the time of fast reproduction only by recording a bit stream on a slanting track as it was especially.

[0005]As a method of the digital video tape recorder which records the above ATV signalsTo the technical announcement in "International Workshop on HDTV'93" held from October 261993 in OttawaCanadaon the 28th. There is "A Recording Method of ATV data on aConsumer DigitalVCR." Hereafterthese contents are described as a conventional example.

[0006]As basic specification of the prototype of a home digital video tape recorderthe recording rate of a digital video signal is set to 25Mbps at the time of SD (Standard Definition) modeWhen field frequency is 60 Hzthere are some which record one frame of an image on the image area of ten tracks. Hereif the data rate of an ATV signal is set to 17-18Mbpstransparent record of an ATV signal will be attained by this SD mode.

[0007]Drawing 30 is a figure showing the head scanning locus of the rotary head at the time of the ordinary reproduction of the conventional digital video tape recorderand fast reproduction. In the figureslanting record of the adjoining track is carried out by turns by the head with a different azimuth angle. Since tape-feed speed is the same as the time of record at the time of ordinary reproductiona head is traceable like drawing 30 (a) along a recording track. Howeverat the time of fast reproductionsince magnetic tape velocity differssome tracks can be crossed and tracedand it can reproduce only the fragment of each same azimuth track. Drawing 30 (b) shows the case of a 5X rapid traverse.

[0008]the bit stream of MPEG 2 -- (-- the bit stream of an ATV signal is mostly based on the bit stream of MPEG 2.) -- only the block by which intra coding was carried out can decode independentlywithout referring to other frames. Supposing the bit stream of MPEG 2 is recorded on each track in orderthe regenerative data at the time of fast reproduction will separate the data by which the Intra numerals were carried out from the regenerative data reproduced intermittentlyand will reconstruct a picture only by the data which was separated [above-mentioned] and by which intra coding was carried out. At this timeon a screenthe area reproduced is not continuation and the fragment of a block will spread on a screen.

Since variable length coding of the bit stream is carried outthe guarantee updated periodically does not have all the screens and there is also a thing with a certain long part which is not done for renewal of time. As a resultit cannot say that the image quality at the time of fast reproduction is enoughand will not be accepted in a home digital video tape recorder.

[0009]Drawing 31 is a block lineblock diagram of the conventional bit stream recorder in which fast reproduction is possible. Hereit divides into the copy areas which record the important portion (H.P. data) of the bit stream which uses the image area of each track for reconstruction of a picture with the main areas which record the bit stream of all the ATV signals at the time of fast reproduction. Since only the intra coding block is effective at the time of fast reproductionthis is recorded on copy areasbut in order to reduce data furthera low-pass frequency component is extracted from all the intra coding blocksand it records as HP data. in drawing 31 -- 1 -- as for a variable length decoder and 5the output terminal of a bit stream and 3 are [a data sampling circuit and 7] EOB (End of Block) additional circuits a counter and 6 the output terminal of HP dataand 4 the input terminal of a bit streamand 2.

[0010]The bit stream of MPEG 2 is inputted from the input terminal 1is outputted as it is from the output terminal 2and is recorded on main areas one by one. On the other handthe bit stream from the input terminal 1 is inputted also into the variable-length decryption machine 4The syntax of the bit stream of MPEG 2 is analyzed and the Intra picture is detectedTiming is generated at the counter 5the low-pass frequency component of all the blocks of the Intra picture is extracted in the data sampling circuit 6furtherEOB is added in the EOB additional circuit 7HP data is constitutedand it records on copy areas.

[0011]Drawing 32 is a figure showing the outline at the time of the ordinary reproduction of the conventional digital video tape recorderand fast reproduction. At the time of ordinary reproductionall the bit streams currently recorded on main areas are reproducedand it is sent to the MPEG 2 decoder out of a digital video tape recorder. HP data is thrown away. On the other handat the time of fast reproductiononly HP data of copy areas is collectedit is sent to a decoderand the bit stream of main areas is thrown away.

[0012]Nextthe arrangement on 1 track of main areas and copy areas is described. Drawing 33 is a head scanning-locus figure at the time of general fast reproduction. If phase lock control of the magnetic tape velocity is carried out by integer double speedhead scanning will synchronize with the same azimuth track. Thereforethe position of the data reproduced is fixed. In a figurewhen the output level of a regenerative signal assumes that a larger portion than -6dB is reproducedthe field to which it added shading by one head will be reproduced. Drawing 33 shows the 9X example and signal read-out of this shaded region is guaranteed in 9X. Thereforewhat is necessary is just to record HP data on this area. Howeverin other double speedsignal read-out is not guaranteedbut it needs to choose this field so that it can read with some magnetic tape velocity.

[0013]Drawing 34 is a figure explaining the area of the overlap at the time of two

or more conventional fast reproduction speedand shows the example of the scan field of three magnetic tape velocity where a head synchronizes with the same azimuth track. Some overlapped ranges are located in the field scanned with each magnetic tape velocity. Copy areas are chosen from these fields and read-out of HP data in different magnetic tape velocity is guaranteed. In drawing 34although the case of 4 times9 timesand 17 times as many rapid traverses is shownthese scan fields become the same as the case of a rapid traverse of -2 twice-7 timeand -15 time.

[0014]It is some magnetic tape velocity and a head is unable to trace the completely same field. That is because the track numbers which a head crosses with magnetic tape velocity differ. It needs to be traceable from every same azimuth track.

[0015]Drawing 35 is a figure of a head scanning locus (5X and 9X) in the conventional digital video tape recorder. By a diagramthe fields 12and 3 are chosen from the overlapped range (5X and 9X). By repeating and recording the same HP data on nine tracks5X HP data [9X] can read either.

[0016]Drawing 36 is two head scanning-locus figures at the time of the 5X reproduction in the conventional digital video tape recorder. As shown in a figureHP data can be read by the head in sync with the same azimuth track by repeating and recording the same HP data as the same track number as magnetic tape velocity. Thereforeby repeating the duplicate of HP data to the same track number as the maximum magnetic tape velocity of fast reproductionduplicate HP data is some magnetic tape velocityand can guarantee read-out for Masakata and in both an opposite direction.

[0017]Drawing 37 is a track arrangement figure in the conventional digital video tape recorderand shows the example of main areas and copy areas. In the home digital video tape recorderthe image area of each track comprised a sink block of 135main areas considered it as 97 sink blocksand copy areas were made into 32 sink blocks. These copy areas have chosen 4 and the overlapped range corresponding to 7 or 17X which were shown by drawing 34. In this casesince the data with about 17.46 Mbps(es) and copy areas same 17 times is recordedthe data rate of main areas is set to about 338.8k bps.

[0018]

[Problem(s) to be Solved by the Invention]Since the conventional home digital video tape recorder is constituted as mentioned aboveit overlaps with the above-mentioned copy areas repeatedly and the data for special reproduction is recorded on them as mentioned aboveIt had the problem that the recording rate of the data for special reproduction was remarkably lowand reproduction image quality was not fully obtained especially in slow reproduction or fast reproduction. For exampleif intra-frame one considers it as a second in two sheets /the data volume of only the intra coding of an ATV signal will be predicted to be about 3 Mbpsbut in a conventional exampleonly about 340K bps can be recorded but reproduction image quality deteriorates dramatically.

[0019]Since only the data by which intra coding was carried out is outputted when

outputting the bit stream (transport packet) of the ATV signal constituted using the data currently recorded on the above-mentioned special reproduction area at the time of special reproductionFor examplewhen there is much intra-frame data volumeit has the problem that the case where a transport packet causes overflow and a system fails in the transmission process of a transport packet in an ATV decoder occurs. The memory space of the memory for special reproduction by the side of reproduction has the problem of becoming large more than needed.

[0020]The composition of the error correcting code of the video-signal area in 1 track of the digital video tape recorder defined by the above-mentioned SD mode (it is hereafter described as SD standard.) and audio signal area is shown in drawing 38. By SD standardas an error correcting code of video-signal areathe Reed Solomon code (it is hereafter described as C1 check code.) of (85779) is used for a recording directionand the Reed Solomon code (it is hereafter described as C2 check code.) of (14913812) is used perpendicularly. The Reed Solomon code (it is hereafter described as C3 check code.) of (1496) is perpendicularly used for the Reed Solomon code [that it is the same as that of a video signal to a recording direction (8577 9)] (C1 check code) as an error correcting code of audio signal area. One sink block (C1 block) which is a record unit of a recording direction is shown in drawing 39. As shown in drawing 39one sink block comprises 90 bytesamong those 5 bytes of a head of a sink pattern and an ID signal are recordedand an error correcting code (C1 detected code) is recorded on back 8 bytes.

[0021]As mentioned aboveat the times of special reproductionsuch as at the time of fast reproductionslow reproductionand still playbacketc.in order that a rotary head may cross a recording track aslanta regenerative signal is reproduced more nearly intermittently than each track. Thereforean error correction block (picture image data) as shown in drawing 38 (a) at the time of special reproduction cannot be constituted. Thereforeat the time of special reproductiononly the error correction by C1 check code is performed to regenerative data.

[0022]When only the error correction by C1 check code is performed and a symbol error rate is 0.01error detection probability becomes $1.56 \times 10^{-3}$and one error will be detected by about 8 sink blocks. Since a reproducing output is not stabilized in particular at the time of special reproductionthe case where a symbol error rate becomes 0.01 or more occurs plentifully. Since variable length coding is performedif an error occursit will become impossible for record data to use subsequent regenerative dataand it will cause degradation of reproduction image quality. It overlooks andalso in an erroroccurrence frequency becomes high dramatically with 7.00×10^{-8}.

[0023]Since only the data by which intra coding was carried out is outputted when outputting the bit stream (transport packet) of the ATV signal constituted using the data memorized in the above-mentioned special reproduction area at the time of special reproductionFor examplewhen there is much intra-frame data volumeit has the problem that the case where a transport packet causes overflow and a system fails in an ATV decoder occurs. The memory space of the memory for

special reproduction by the side of reproduction has the problem of becoming large more than needed.
[0024]The purpose of this invention is as follows.
It was made in order to solve the above problemsand improve the reproduction image quality at the time of slow reproduction or fast reproduction especially. Interface control can be performed so that the control by the side of an ATV decoder may not be different from the time of ordinary reproduction at all at the time of special reproduction (at the time of fast reproductionslow reproductionand still playback)Reduce the memory space at the time of fast reproductionand obtain the digital signal playback equipment which can perform fast reproduction efficiently.

[0025]
[Means for Solving the Problem]Digital signal playback equipment concerning claim 1 of this inventionthe inside of a frame or the field inputted in the state of a packet -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outData for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn digital signal playback equipment in which data for special reproduction generated [above-mentioned] reproduces a recording medium currently recorded on a positionA data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand a still picture slice data generating means in which all the macro blocks in a slice generate slice data whose prediction error a motion vector is 0 in 0After outputting one frame separated from said data storage meansor the above-mentioned data for special reproduction for the 1 fieldit constitutes so that predetermined carries out the frame number partial output of the output of the above-mentioned still picture slice generating means and the above-mentioned still picture slice generating means may be controlled.
[0026]Digital signal playback equipment concerning claim 2 of this inventionthe inside of a frame or the field inputted in the state of a packet -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outData for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn digital signal playback equipment in which data for special reproduction generated [above-mentioned] reproduces a recording medium currently recorded on a positionA data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand

a still picture slice data generating means in which all the macro blocks in a slice generate slice data whose prediction error a motion vector is 0 in 0The above-mentioned data for special reproduction separated from regenerative data reproduced intermittently by the above-mentioned data separation means 1 or plural slicesWhile constituting a transport packet for one **** for an output of a still picture slice data generating meansthe above-mentioned transport packet And the fieldOr a packet is constituted so that data for special reproduction which considered it as a packet in inter-frame-prediction modeand was reproduced by the above-mentioned intermittent target may be made into the compulsory intra-frame mode and may be transmitted.

[0027]At the time of still playbackdigital signal playback equipment concerning claim 3 of this invention constitutes so that an output in the above-mentioned still picture packet creating means may always be chosen after an end of a final data output of the above-mentioned frame or a frame reproduced at the time of ordinary reproduction.

[0028]Digital signal playback equipment concerning claim 4 of this inventionIt constitutes so that an output of the above-mentioned still picture packet creating means may be chosenand the above-mentioned data switching means may be controlleduntil a servo system locks and intra-frame data for [above-mentioned] special reproduction is reproduced from the above-mentioned fast reproduction area at the time after the mode to fast reproduction.

[0029]Digital signal playback equipment concerning claim 5 of this invention is constituted so that the above-mentioned control system may be used at least at the time of special reproduction of an opposite direction.

[0030]Digital signal playback equipment concerning claim 6 of this inventionthe inside of a frame or the field inputted in the state of a packet -- orWhile transparent record of a frame or a digital video signal by which interfield coding was carried outand the digital audio signals is carried outData for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn digital signal playback equipment in which data for special reproduction generated [above-mentioned] plays magnetic tape currently recorded on a positionWhen a data separation means which separates the above-mentioned data for special reproduction from a regenerative signaland data outputted from a digital signal recording and reproducing device are decoded and reproduced image data is restoredWhen it has a specific area fixed packet creating means which generates a packet for standing a signal of specific area on a screen still and a reproduced image is constituted using data reproduced intermittently at the time of special reproductionan output of the above-mentioned specific packet fixing meansThe above-mentioned regenerative data is switchedand it constitutes so that the above-mentioned data for special reproduction of one frame may be divided into a multiple frame and may be transmitted.

[0031]

[Function]In the digital signal playback equipment concerning claim 1 of this inventionthe inside of the frame or the field inputted in the state of the packet -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium currently recorded on the positionThe data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand a still picture slice data generating means in which all the macro blocks in a slice generate the slice data whose prediction error a motion vector is 0 in 0Since it constitutes so that predetermined may carry out the frame number partial output of the output of the above-mentioned still picture slice generating meansand the above-mentioned still picture slice generating means may be controlled after outputting one frame separated from said data storage meansor the above-mentioned data for special reproduction for the 1 fieldWhile being able to reduce memory space and being able to aim at reduction of circuit structurespecial reproduction can be realized without making an ATV decoder conscious of special reproduction mode.

[0032]In the digital signal playback equipment concerning claim 2 of this inventionthe inside of the frame or the field inputted in the state of the packet -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium currently recorded on the positionThe data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand a still picture slice data generating means in which all the macro blocks in a slice generate the slice data whose prediction error a motion vector is 0 in 0The above-mentioned data for special reproduction separated from the regenerative data reproduced intermittently by the above-mentioned data separation means 1 or plural slicesWhile constituting the transport packet for one frame using the output of a still picture slice data generating meansthe above-mentioned transport packet And the fieldOr since a packet is constituted so that the data for special reproduction which considered it as the packet in inter-frame-prediction modeand was reproduced by the above-mentioned intermittent target may be made into the compulsory intra-frame mode

and may be transmittedthe memory space at the time of fast reproduction can be reducedand circuit structure can be reduced.
[0033]In the digital signal playback equipment concerning claim 3 of this inventionSince the output in the above-mentioned still picture packet creating means is constituted after the end of a final data output of the above-mentioned frame or frame reproduced at the time of ordinary reproduction at the time of still playback so that it may always outputIt is not necessary to provide the memory which stores the Intra information for one frame in the digital video tape recorder side also in the still playback which does not use the data for special reproductionand a good reproduced image can be constituted by using the still picture packet creating means used at the time of fast reproduction.
[0034]In the digital signal playback equipment concerning claim 4 of this inventionUntil a servo system locks and the intra-frame data for [above-mentioned] special reproduction is reproduced from the above-mentioned fast reproduction area at the time after the mode to fast reproductionSince it constitutes so that the output of the above-mentioned still picture packet creating means may be chosenand the above-mentioned data switching means may be controlledmode transition can be performed smoothlywithout disturbing a reproduced image at the time of mode transition.
[0035]In the digital signal playback equipment concerning claim 5 of this inventionthe data provided in reverse direction reproduction arrangingand changingwhile the memory space at the time of fast reproduction is reduciblesince it constitutes so that the above-mentioned control system may be used at least at the time of the special reproduction of an opposite direction -- business -- a memory becomes unnecessary and the further circuit structure can be reduced.
[0036]In the digital signal playback equipment concerning claim 6 of this inventionthe inside of the frame or the field inputted in the state of the packet -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium currently recorded on the positionWhen the data separation means which separates the above-mentioned data for special reproduction from a regenerative signaland the data outputted from the digital signal recording and reproducing device are decoded and reproduced image data is restoredWhen it has a specific area fixed packet creating means which generates the packet for standing the signal of the specific area on a screen still and a reproduced image is constituted using the data reproduced intermittently at the time of special reproductionthe output of the above-mentioned specific packet fixing meansSince it constitutes so that the above-mentioned regenerative data is switchedand the above-mentioned data for special reproduction of one frame may be divided into a multiple frame and may be

transmittedThe memory space at the time of fast reproduction is reducible.
[0037]
[Example]
Example 1. drawing 1 is a block lineblock diagram of the reversion system of the digital video tape recorder which is one example of this invention. In a figurea rotating drumand 20a and 20b 19 A rotary headThe signal detection circuit where 21 detects a head amplifier and 22 detects digital data from a regenerative signalThe digital demodulation circuit where 23 performs digital demodulation to the reproduction digital data outputted from the signal detection circuit 22The ID detection circuit where 24 detects an ID signal from the above-mentioned digital demodulation signal25 the error contained in the regenerative signal with which digital demodulation was performed using the C1 above-mentioned check code (error correcting code of a recording direction) An error correctionThe 1st error correction decoding circuit that carries out error detectionand 26 At or the time of ordinary reproduction. the data (the data by which error detection was carried out.) by which an error correction was not carried out with C1 check code Use C2 check code (error correcting code added to the perpendicular direction of the video signal) for the data which overlooked the errorand Or an error correctionOr the error correcting code with which the 2nd error correction decoding circuit that performs error detectionand 27 are added to the 3rd memoryand 28 is added to the data for special reproduction (it is hereafter described as C4 check code.) Details about C4 check code are given later. Use and Error correctionThe 3rd error correction decoding circuit that performs error detectionand 29 Or the 4th memoryA switch and 33 are the output terminals of data the still picture packet generating circuit where 30 generates a still picture packet based on the control signal outputted from the 3rd memory 27 or the 4th memory 29and 31 and 32.
[0038]Hereafterbefore explaining the contents of this example 1the ID signal used for a digital video tape recorder etc. is explained briefly. An error correcting and detecting code for the ID signal of the digital video tape recorder described by SD standard to correct or detect additional informationsuch as a track number and a sink block numberand the error contained in an ID signal at the time of reproduction is recorded. This is a dropout etc. at the time of ordinary reproductionand when the information on a number sink block is missingit is used as an auxiliary signal for memorizing the data of the sink block reproduced correctly immediately after a dropout to the predetermined address in 1 error correction block shown in above-mentioned drawing 38. At the time of special reproductionsuch as fast reproduction and slow reproductionit is used as a reference signal in the case of writing address generating to the memory 40 (the details of the memory 40 are mentioned later.) of the data of a reproduction sink block. In this example 1the error detecting code which detects the above-mentioned track numberthe sink block number in a trackand the error generated in an ID signal at the time of reproduction as an ID signal shall be recorded.
[0039]Drawing 2 is a block lineblock diagram of the 3rd error correction decoding circuit 28 which is one example of this invention. (In additionalthough the 2nd error

correction decoding circuit 26 also differs in the size of each memoryit takes an identical configuration fundamentally.) In a figureThe renewal flag memory of data in which 40 stores a memory in and 41 stores the update flag of regenerative dataThe update flag memory control circuit where 42 controls the above-mentioned renewal flag memory 41 of dataThe error correction circuit which performs an error correction to the data into which 43 was inputtedthe error correction control circuit where 44 controls the memory 40the renewal flag memory 41 of datathe update flag memory control circuit 42and the error correction circuit 43The input terminal of the ID information to which 45 is outputted from the input terminal of regenerative dataand 46 is outputted from the ID detection circuit 24and the error detection flag of an ID signalthe output terminal of the data in whichas for 47the error correction was performedand 48 are the output terminals of an error detection flag. The details of the above-mentioned update flag data are mentioned later.

[0040]Drawing 3 is a block lineblock diagram of the error correction circuit 43 which is one example of this invention. After 50 generates syndrome in a figure from the data read from the memory 40The error correction core circuit which corrects or detects the error in regenerative data based on syndrome (in addition) the error correction of the data stored in the memory 40 is also performed in the error correction core circuit 50. The error correction core control circuit which generates the control signal which controls the error correction core circuit 50 based on the control signal with which 51 is outputted from the error correction control circuit 44The compulsive IREJA flag storage memory 52 remembers the data update flag position outputted from the renewal flag memory 41 of data to beThe error correction decoding according [53] to the 1st 25Cerror correction decoder 1 check code. (It is hereafter described as C1 decoding.) It is C4 error-detection flag storage memory which memorizes the error position detected at C1 error-detection flag storage memory which memorizes the sometimes detected error positionand the time of the error correction decoding (it is hereafter described as C4 decoding.) by 54C4 check code.

[0041]Based on the control signal outputted55 from the error correction core control circuit 51 The writing of the data to the above-mentioned compulsion IREJA flag storage memory 52C1 error-detection flag storage memory 53and C4 error-detection flag storage memory 54And the flag memory control circuit which generates the read-out control signal of dataThe error detection flag generation circuit which generates the error detection flag which 56 adds to the data which detected the errorThe error detection flag memory 57 remembers the above-mentioned error detection flag outputted from the error detection flag generation circuit 56 to beThe input terminal of a data update flag in which 58 is outputted from the renewal flag memory 41 of dataThe input/output terminal in which 59 communicates the memory 40 and dataand 60 The input/output terminal of a control signal with the error correction control circuit 4461 is an output terminal which outputs the data read from the error detection flag memory 57 to predetermined timing based on the control signal outputted from the error

correction core control circuit 51. The regenerative data in which the error correction was performed is inputted into the 4th memory 29 via the output terminal 47 from the memory 40.

[0042]Drawing 4 is a figure showing arrangement of the data in 1 track which is one example of this invention based on SD standard. Arrangement of the rotary head 20 (a) on the typical drawing 5 (a) rotating drum 19 used for - (c) at the time of the above-mentioned SD mode and the rotary head 20 (b) is shown. Drawing 6 is a figure showing the data packet which is one example of this inventiondrawing 6 (a) shows the transport packet contained in an input bit streamand drawing 6 (b) shows the recording data packet recorded on magnetic tape. Drawing 7 is a code configuration figure of the error correcting code added to the data for special reproduction of the digital video tape recorder which is one example of this invention. Drawing 8 is a figure showing the number of sink blocks in which the data acquisition at the time of fast reproduction is possible. Drawing 9 is a plot plan of the data recording area for special reproduction in the track of the digital video tape recorder which is one example of this inventionand a figure showing arrangement of the data recording area for special reproduction. Drawing 10 is a figure showing the split method of 1 error correction block of the 16X (-14 X) data of the digital video tape recorder which is one example of this invention. Drawing 11 is a figure showing the track format of the digital video tape recorder which is one example of this invention. Hereafterbefore explaining operation of the reversion system of this inventiondrawing 4 - drawing 11 are used and the recording format of this example 1 is explained briefly.

[0043]The transport packet inputted at the time of record (the contents) It comprises a digital video signaldigital audio signalsdigital data concerning a video signal and an audio signal furtheretc. As shown in drawing 6 (a)it comprises 4 bytes of a header unitand 184 bytes of a data division.

[0044]On the other handalthough SD standard described also by the conventional exampleone sink block comprises 90 bytesas shown in drawing 39among those 5 bytes of a head of a sink pattern and an ID signal are recordedand an error correcting code (C1 check code) is recorded on back 8 bytes. Thereforedata memorizable in 1 sink block will be 77 bytes as shown in a figure. Thereforein this example 1from a bit streama transport packet shall be detectedand two detected transport packets shall be changed and recorded on the record data block of five sink blocksas shown in drawing 6 (b). In a figureH1 is the 1st header and H2 is the 2nd header. The flag etc. which identify whether they are identification data in which it is shown the sink of what position of five sink blocks it isand data for special reproductionor it is data for ordinary reproduction are recorded on H1. Picture image datathe identification data of audio information etc.etc. is recorded on H2. 149 sink blocks of recording area of the data in 1 track are prepared as area which records picture image data around one track as shown in drawing 4although the conventional example also described. 11 blocks as VAUX data recording area are provided for the inner 3 block as error correcting code recording area (C2 check code).

[0045]Nextthe data recording area for special reproduction on magnetic tape is explained using drawing 7 - drawing 11. The number of sink blocks which can be acquired from one track at each fast reproduction speed was shown in drawing 8. In a figurea 9000-rpm system shows the system of the head arrangement shown in drawing 5 (a) and drawing 5 (b)and a 4500-rpm system is with what shows the system of the head arrangement shown in drawing 5 (c). When each value in a figure performs special reproduction using a 10 micrometers (the track pitch in SD standard is 10 micrometers in addition.) rotary headit shows the number of sink blocks renewable from one track at each reproduction speed. Calculation made the number of sink blocks of one track (180 degrees) 186 sink blocksand it computed ithaving assumed it to be that from which a portion with a larger output level of a regenerative signal than -6dB is obtained like a conventional example.

[0046]In consideration of the number of sink blocks which is shown in drawing 8 and in which data acquisition is possiblearrangement of the data recording area for special reproduction in the track of the digital video tape recorder in this example 1 was shown in drawing 9 (a). The data recording area for special reproduction is repeated 4 track cyclesandas for this recording formatthe data recording area for special reproduction corresponding to each double-speed number is provided on four above-mentioned tracks. The inside a1 and a2 of a figure as area which records the data for special reproduction 2X4Xand for -2 Xc1 and c2 as area where b1 and b2 record the data for special reproduction 8X and for -6 X are provided as area which records the data for special reproduction 16X and for -14 X. An ATV signal shall be recorded on other area (it is hereafter described as ATV data recording area.).

[0047]The data (the number of sink blocks) recorded on each data recording area for special reproduction was shown in drawing 9 (b). Identical signals shall be recorded on the area in which the identical codes in a figure were described. (For examplethe data of one in a1 is recorded also on the portion of one in a2.) About a1 and a2 areathe same data is recorded repeatedly twiceand the same data is repeatedly recorded again about b1 and b2 area 4 times. About c1 and c2 areaas shown in drawing 10five sink blocks are quadrisected for the data for special reproduction (1 error correction block) in which the above-mentioned error correcting code was added as a unitAfter repeating two upper blocks 8 times and recording themthe block of the two bottoms is repeated 8 times and recorded. The arrangement on the detailed magnetic tape of each data recording area for special reproduction is shown in drawing 11. The same data for special reproduction will be recorded on the area (A1A1'B1B1'C1C1'etc.) in which identical codes were described among a figure.

[0048]The operation at the time of special reproduction is briefly explained using drawing 8. In a 4500-rpm systemonly 31 sink blocks are renewable to 62 sink block data being more nearly renewable in 4X from one track in a 9000-rpm system than in drawing 8. That isby this recording formatall the data for special reproduction currently recorded on the track of a1 is renewable in a 9000-rpm system at the time of 4X reproduction (.).That isall the signals (the area described as ECC is also

included among a figure.) of 123and 4 which are shown in drawing 9 (b) are renewable. Since about nine sink blocks are not reproduced1 error correction block shown in drawing 7 cannot consist of 4500-rpm systems. (That iswith the number sink block data of the head of the portion of one in drawing 9 (b).) The number sink block data of the last of the portion of 4 is not reproduced. Thereforeit constitutes from a digital video tape recorder shown in Example 1 of this invention so that the ancillary data used for a2 portion at the time of a 4500-rpm system may be recorded. (The above-mentioned 1 error correction block is constituted using the data currently reproduced from the rotary head of 19 (b) which adjoined about the constitution method of 1 error correction block at the time of the special reproduction in a 4500-rpm systemand has been arranged.) Since it differs from the main point of this invention for detailsit omits.

[0049]Hereaftera recording format is explained. The bit stream of the ATV signal compounded by the sync block unit as shown in drawing 6 (b) is recorded on the recording area of an ATV signal. On the other handthe data for special reproduction is generated from intra-frame (inside of a frame or data formed into the field inner code (intra coding) in the bit stream of MPEG 2) one separated out of the bit stream. In this example 1the data for special reproduction shall be generated from intra-frame one which is respectively different by the double-speed number set up beforehand. Hereafterit is the refresh time at the time of 8X reproduction and 16X reproduction (at the above-mentioned reproduction speed) at the time of the 4X reproduction in the recording format shown in above-mentioned drawing 9. If the minimum time when a reproduced image is updated is carried out for 0.5 second when a special reproduction picture is constituted using the data currently recorded on the above-mentioned special-reproduction-data recording areaBy 4X reproductionit can be set to about 0.66 Mbit by about 1.32 Mbit and 8X reproductionit will be about 0.33 Mbit at 16Xand the code amount of the special reproduction picture which constitutes one at each speed can act as Kougami of the reproduction image quality at the time of each double speed at the time of special reproduction compared with a conventional example. Hereafterthe code amount in each double-speed number is explained as what assigned the above-mentioned code amount.

[0050]Data volume is respectively reduced so that variable-length decoding may be given and the data which was separated from the inputted bit stream and by which intra coding was carried out may become the above-mentioned code amount. the data of each above in which data volume was reduced is compounded againand the transport packet which header information etc. are added and is shown in drawing 6 (a) is constituted. And the record data block which collects the two above-mentioned transport packets and is shown in the figure (b) is constituted. And the three above-mentioned record data blocks are collected1 error correction block is constitutedand after adding C4 check code shown in drawing 7C1 check code is added.

[0051]As C4 check codethe Reed Solomon code of (20156) shall be adopted by this example 1. By that which constitutes 1 error correction block for special

reproduction shown in drawing 7 from this example 1 at the time of special reproductionand performs an error correction to regenerative data (the error correcting code by C4 check code is given to the data to which an error correction was not performed by C1 check code). It is set to the level on which about 10^{10} double error detection probability is improved and which error detection probability in case a symbol error rate is 0.01 serves as a 1.54×10^{-13} gradeand is satisfactory practically. It overlooks and an error is also set to a 2.38×10^{-16} grade and the level which is satisfactory practically. As long as the case where a symbol error rate becomes 0.01 or more at the time of special reproduction occurs plentifully as the conventional example also describedbut the calculation result about an error rate is seenit is set to the level which is satisfactory practically by the above-mentioned code configurationand a good special reproduction picture can be acquired.

[0052]Based on the abovethe recording format of this example 1 is explained below. The bit stream of the inputted ATV signalTwo transport packets comprise five sink blocks as mentioned aboveand it is recorded on area other than the data recording area for special reproduction on the ATV data area (referring to drawing 4 and the following describe this area as main areas.) on the above-mentioned recording track by making one sink block into a unit.

[0053]On the other handthe data for special reproduction for each double speed of the 20 above-mentioned sink block to which the error correcting code was added is recorded on the corresponding data recording area for special reproduction shown in drawing 9 (a). Prescribed frequency repetition record of the data for special reproduction corresponding to each double-speed number is carried out as mentioned above. In the case of the data for 4X reproductionas shown in drawing 9 (b)specificallyit is 2 times (in additionin the case of a1 areaone error correction block is constituted from the first 20 sink blocksand it constitutes another error correction block from 20 sink blocks of the second half.). that isthe contents differ in the error correction block of the first halfand the error correction block of the second half. In the case of the data for 8X reproduction4 timesin the case of the data for 16X reproductionas shown in drawing 101 error correction block is divided into ten sink blocks of the first halfand ten sink blocks of the second halfAfter repeating the data of ten sink blocks of the first half 8 timesthe data of ten sink blocks of the second half is repeated 8 timesand is recorded.

[0054]About refreshment of the data for special reproduction corresponding to each double-speed numberit shall be carried out with a predetermined cycle as mentioned above. this example -- one -- **** -- every 2 secondsevery 4 seconds8X extracts the 16X Intra picture from an input bit stream every 8 secondsand updates the 4X picture for special reproduction. About the cycle of refreshmentit does not restrict to this. The recording format of this example 1 is shown in drawing 11.

[0055]Hereafteroperation of the reversion system of a digital video tape recorder which has the above recording formats is explained using drawing 1 - drawing 3. It begins first and ordinary reproduction operation is explained. At the time of

ordinary reproductionafter the data played via the rotary heads 20a and 20b from magnetic tape is amplified with the head amplifier 21signal detection is performed in the signal detection circuit 22and it is changed into playback digital data. The synchronized signal added to the head of each sink block in that case is detected. As for the reproduction digital data outputted from the signal detection circuit 22digital demodulation is performed in the digital demodulation circuit 23. The data in which digital demodulation was performed is inputted into the ID detection circuit 24 and the 1st error correction decoding circuit 25. In the ID detection circuit 24the ID signal added to the head part of each sink block on the basis of the synchronized signal detected in the signal detection circuit 22 is separatedand the error contained in an ID signal using the error detecting code added to the ID signal is detected. On the other handin the 1st error correction decoding circuit 25correction of the error which was with C1 check code added to the recording directionand was generated in the regenerative signaland detection are performed. The data in which the error correction was performed is inputted into the 2nd error correction decoder 26 and the 3rd error correction decoder 28.

[0056]the data (the data by which error detection was carried out.) by which an error correction was not carried out with the C1 above-mentioned check code in the 2nd error correction decoder 26 Or C2 check code (error correcting code added to the perpendicular direction of the video signal) is used for the data which overlooked the errorand an error correction or error detection is performed (it is hereafter described as C2 decoding.). The data in which C2 decoding was given is inputted into the 3rd memory 27. By the 3rd memory 27the bit stream of an ATV signal is separated from the inputted dataand only the above-mentioned bit stream is memorized in a memory. (The data for special reproduction is thrown away like a conventional example in this stage.)

[0057]On the other handthe data inputted into the 3rd error correction decoder 28 is begun firstand 1 error correction block which the data for special reproduction currently recorded on the above-mentioned data recording area for special reproduction is separated from regenerative dataand is shown in drawing 7 is constituted. Separation of the data recording area for special reproduction detects the position of the data recording area for special reproduction on a track by the sink block number currently recorded into the ID signal in a sink blockIt is distinguished by detecting the header in a sink block whether it is data for special reproductionor it is a bit stream of the usual ATV signal.

[0058]When the data of the above-mentioned 1 error correction block is constitutedin the 3rd error correction decoder 28. C4 check code (error correcting code added to the perpendicular direction of the data for special reproduction) is used for the data (data by which error detection was carried outor data which overlooked the error) by which an error correction was not carried out with the C1 above-mentioned check codeand an error correction or error detection is performed. The data in which C4 decoding was given is inputted into the 4th memory 29. It explainswhen explaining the operation at the time of fast reproduction about the details of operation of the 3rd error correction decoding

circuit 28.
[0059]In this example 1the shortest distance of C4 check code of the data for special reproduction and the shortest distance of C3 check code of audio information are designed identically. Since the audio signal of an ATV signal is transmitted with a digital video data into the bit stream of an ATV signal as the conventional example also describedthis will not be recorded on audio signal areabut it will be recorded on video-signal area together with a video signal. Thereforewhen reproducing the digital video tape recorder which recorded the ATV signalthe error correction decoding circuit for audio signals will be used. In this example 1reduction of circuit structure is aimed at by sharing the 3rd error correction decoder 28 with the error correction decoder of an audio signaland using it by making the same the shortest distance of C4 check codeand the shortest distance of C3 check code as mentioned above.
[0060]By the 4th memory 29the inputted data for special reproduction in which the error correction was performed is memorized in a memory. At the time of ordinary reproductionthe switch 32 is constituted so that the output of the 3rd memory 27 may always be chosenand the bit stream of ATV restored to 188 bytes of packet information by the 3rd memory 27 is outputted from the output terminal 33.
[0061]Nextstill mode is explained. Still playback has two casesthe case where it shifts to still modeand when still mode is chosen from a halt conditionduring ordinary reproduction. It begins first and the case where it shifts to still mode from ordinary reproduction operation is described. If still mode is chosen from ordinary reproductionregenerative data will be stopped and data will no longer be inputted into the 3rd memory 27 and the 4th memory 29. Thereforean input of a still mode signal will detect the end of the frame data of the regenerative data of an ATV signal from a regenerative signal in the 3rd memory 27. Intra-frame one or a prediction frame may be sufficient as this. If the end of the above-mentioned frame data is detectedthe 3rd memory 27 will output the end detecting signal of frame data to the still picture packet generating circuit 30. At this example 1the end of the above-mentioned frame data shall be detected with the output of the 3rd memory 27.
[0062]In the still picture packet generating circuit 30an input of the end detecting signal of the above-mentioned frame data will generate the transport packet which shows that it is a still picture. Hereafterbefore beginning concrete explanationthe composition of the image data of one frame specified by MPEG 2 is described briefly.
[0063]In MPEG 2DCT blocks (eight lines x 8 pixels) are made into the minimum unit of the processing at the time of high efficiency coding. And the two or more blocks above-mentioned DCT blocks are collectedand a macro block is constituted. The macro block serves as a unit which detects a motion vector. With a slicethese two or more blocks macro blocks are collectedand it is constituted. By MPEG 2it is defined as constituting the above-mentioned slice from data in the same horizontal blocks of a macro blockand does not limit for the macro block

number contained in it. The DCT blocks (eight lines x 8 pixels) of two color-difference signals with which the macro block in an ATV signal has DCT blocks of a luminance signal in the same position on four pieces (16 lines x 16 pixels)and it and a screen comprise every one piece each. By an ATV signalimage data is sent in the form of 4:2:0. (see the written standards of MPEG 2 for details)

[0064]In consideration of the above-mentioned thingthe contents of the transport packet which shows that it is the above-mentioned still picture outputted from the still picture packet generating circuit 30 are explained. By this example 1a motion vector collects the two or more blocks transport packets whose prediction error signals are 0 by 0and the data in the above-mentioned macro block specifically generates slice dataOne slice or a plural-slices collection transport packet is generated for this slice data. (This transport packet is hereafter described as a still picture packet.) Again in the still picture packet generating circuit 30. The packet which shows no data that the frame period in an ATV decoder suits with the above-mentioned still picture packet is generatedand a transport packet is generated so that the frame period in an ATV decoder may suit combining these two packets.

[0065]The motion vector of all the macro blocks which belong in a slice as the one example in this example 1 by 0. The transport packet from which all the data in all the DCT blocks in the above-mentioned macro block collected one or more slices which are 0 (that isDC data comprises 0 and AC data comprises only EOB (end of block).)and constituted them shall be shown. A no data packet is a packet which means that it is the transport packet defined by the bit stream of the ATV signaland this packet information is a packet which does not have a meaning as transmitted data. If a transport header portion defines a no data packetthe data in the transport packet which continues henceforth will be disregarded at the time of decoding by an ATV decoder. Namelyin the still picture packet generation circuit 30the data part in a transport packet always generates the information on an above-mentioned still picture packetThe header unit which judges whether it is a no data packet which the change of an output is added by the prescribed position of a transport headerand is transmitted is switched and generated. Therebyreduction of the circuit structure of the still picture packet generating circuit 30 can be aimed at.

[0066]In the switch 31an input of a still mode signal will choose the output of the still picture packet generating circuit 30. The switch 32 is controlled to choose the output of the switch 31 based on the terminate signal of the frame data of the above-mentioned ATV signal outputted from the 3rd memory 27. Although the end of the above-mentioned frame data is detected from the output data of the 3rd memory 27it does not restrict to thisand even if specified quantity delay is detected and carried out in the input of the 3rd memory 27 and it controls the above-mentioned still picture packet generating circuit 30 and the switch 32 by this example 1for examplethe same effect is done so by it. It cannot be overemphasized that the above-mentioned data switching timing may be switched in the position which detected the intra-frame final packet. (Since some are better

than the image quality of a reproduced image consists of inter-frame data when a still picture is constituted from intra-frame oneit is effective.)
[0067]Nextthe case where still mode is chosen from a halt condition is described. Since right data is not transmitted [a halt condition] to the receiving set (decoder) side of ATVwhen still mode is chosen in this stateWhat is necessary is for the above-mentioned switches 31 and 32 and stillness to control the packet generating circuit 30 by an above-mentioned wayand just to suspend a tapeafter playing once and sending the data for one screen to the receiving set side of ATV. In this casethe end position of intra-frame data is detected and it controls by the 3rd memory 27 to output the terminate signal of the above-mentioned frame data. This is because a reproduced image cannot be constituted with a motion vector since only the prediction error ingredient is transmitted even if it detects an inter-frame frame terminate signal.
[0068]In above-mentioned Example 1although the ATV signal used at the time of ordinary reproduction is used as data for still playbacksit does not restrict to thisand even if it performs same control using the data for special reproduction memorized by the 4th memory 29the same effect is done so. (If a still mode signal is inputtedthe switch 32 will choose the output of the switch 31.) After the switch's 31detecting the end of the frame data outputted from the 4th memory 29 on the other handThe output of the still picture packet generating circuit 30 is chosen. When an error is detected in the ATV signal especially used for the above-mentioned ordinary reproductiongood still playback can be realized by using the above-mentioned data for special reproduction. It shall constitute from this example 1 so that the data of the transport packet reproduced from the data recording area for special reproduction used at the time of most 2X4Xand - 2X reproduction of record data volume at the time of still playback may be outputted. (Thereforesince the data used at the time of still playback should just be decoded at the time of ordinary reproduction) It may constitute from the 3rd error correction decoding circuit 28 so that only the 2 above-mentionedX4Xand the data recording area for special reproduction used at the time of - 2X reproduction may be decoded. By the above composition. While being able to realize still playback by easy circuitrywithout making still playback mode recognize to the ATV decoder sidewhen an error is detected in a regenerative signalgood still playback can be realized by using the data currently recorded on the above-mentioned special-reproduction-data recording area. By the above-mentioned compositionthe memory space of the 3rd memory 27 is reducible to about 4 track x2 by this example 1. (In addition by the formerthe memory space for one intra-frame frame was needed.)
[0069]Nextthe operation at the time of fast reproduction is explained. This example 1 explains the case of the composition of the rotary head shown in drawing 5 (a). Drawing 12 is a scanning-locus figure of the rotary head 20a at the time of performing the twice which is one example of this invention4 times8 timesand 16X reproduction. The scanning locus of the rotary head 20a shown in drawing 12 takes a locus also with same composition of the rotary head shown in

drawing 5 (b). (Howeversince head arrangement differs about the rotary head 20 (b)it becomes a locus which is completely different.) Drawing 13 is an explanatory view of operation for explaining the tracking control operation of the digital video tape recorder which is one example of this invention. Firstthe tracking control method at the time of the fast reproduction in this example 1 is explained using drawing 12 and drawing 13. At the time of fast reproductiondata is reproduced intermittently as mentioned above. The number of sink blocks renewable from one track at each reproduction speed comes to be shown in drawing 8.

[0070]thereforewhat is necessary is just to control the tracking of the rotary head 20 (a) so that a reproducing output becomes the maximum at the center of area that the above-mentioned data for special reproduction is recorded in each double-speed number in order to acquire the data for special reproduction effectively Drawing 13 (a) The tracking control point of the rotary head 20 at each reproduction speed (a) was shown in - (c). In the recording format shown in this example 1since the data of 1 error correction block shown in drawing 7 was constituted from a 9000-rpm system even if it did not use the data reproduced from the rotary head 20 (b)at drawing 12it omitted about the scanning locus of the rotary head 20 (b).

[0071]Based on the above thingoperation of the reversion system at the time of fast reproduction is explained using drawing 1 - drawing 3drawing 12and drawing 13. If the mode signal of fast reproduction is inputtedthe switch 32 will choose the output of the switch 31. (The timing that in addition a switch-off substitute is fine is mentioned later.) The rotary head 20aAnd after the regenerative data intermittently reproduced via 20b is amplified with the head amplifier 21it is changed into reproduction digital data in the signal detection circuit 22and digital demodulation is performed in the digital demodulation circuit 23. Data right and detected in the signal detection circuit 22 is inputted into the ID detection circuit 24 and the 1st error correction decoding circuit 25. In the ID detection circuit 24the ID signal added to the head part of each sink block on the basis of the synchronized signal detected in the signal detection circuit 22 is separatedand the error contained in an ID signal using the error detecting code added into the ID signal is detected.

[0072]On the other handin the 1st error correction decoding circuit 25correction of the error which was with C1 check code added to the recording directionand was generated in the regenerative signaland detection are performed. (C1 decoding) The data in which the error correction was performed is inputted into the 3rd error correction decoder 28. The output of the 1st error correction decoding circuit 25Although inputted also into the 2nd error correction decoding circuit 26since data is reproduced intermittently as mentioned aboveC2 decoding cannot be performed and a transport packet cannot be generatedin this example 1C2 decoding operation shall not be performed at the time of fast reproduction. Hereafterbefore explaining operation of the 3rd error correction decoding circuit 28the general error correction decoding algorithm of the error correcting code of the product-code form shown in drawing 7 or drawing 38 is explained briefly.

Drawing 14 is a figure explaining general C1 decoding algorithm used for a digital video tape recorder. Drawing 15 is a figure explaining general C4 decoding algorithm used for a digital video tape recorder. GenerallyC2 decoding and C3 decoding algorithm are also decoded with the same algorithm as C4 decoding algorithm shown in drawing 15 only by the shortest distance differing from code length.

[0073]Reproduction of data will perform correction of the error first generated in the regenerative signal using C1 check code to the limit of the error correction capability which C1 check code has. The algorithm of C1 decoding is shown in drawing 14. If it begins first and C1 decoding is startedsyndrome will be generated using the data outputted from the digital demodulation circuit 23. Calculation of an error position and a numerical value is performed using the syndrome generated after generation of syndrome was completed. When an error position and a numerical computed resultand the error number are four or less piecesan error correction is performedand when the error number is judged to be four or more piecesan error detection flag is outputted. (The above-mentioned error detection flag is hereafter described as an IREJA flag.) In additionby this example 1since the shortest distance of C1 check code is 9it corrects to a maximum of four errors.

[0074]As for the error which was not able to perform an error correction with C1 check codean error correction is performed using C4 check code. The error correction by C4 check code in this example 1 performs an error correction to overlooking by C1 check code while performing disappearance correction (it is hereafter described as IREJA correction.) to the error detected by C1 check code. HereafterC4 decoding ****** explanation is given based on the decoding algorithm shown in drawing 15.

[0075]The number of IREJA counts based on the above-mentioned IREJA flag with which the data of 1 error correction block shown in drawing 7 is constituted in the memory 40 and which was detected by C1 check code while it was not rich and syndrome was generated at first using input data. When the number of IREJA is below the correcting capability of C4 check code (since the shortest distance of C4 check code of this conventional example is 6) Correction is possible to a maximum of five IREJA. Based on the syndrome generated [above-mentioned]IREJA correction is performed to the error detected by C1 check code in quest of correction syndrome. (In additionsince it changes with decoding algorithmswhen using algorithms other than Euclid decodingthe method of disappearance correction) Correction syndrome shall not be searched for but syndrome and an IREJA position shall perform disappearance correction by other methods. In that casean error correction is performed to the limit of error correction capability also about the overlooking error by C1 check code. On the other handwhen the number of IREJA detected by the C1 above-mentioned check code is over correcting capabilityit carries out to the limit of error correction capability that do not search for correction syndrome but C4 check code has an error correction as it is (a maximum of two errors are corrected.). Since this has the high probability that the error detected by C1 check code is empty IREJA

(although error detection was carried out by C1 check codewhen it is an exact value in practice)it becomes possible to perform an error correction.
[0076]The time of the fast reproduction which appears especially notably the problem at the time of performing an error correction and detection using the abovedrawing 14and the decoding algorithm shown in drawing 15 is made into an exampleand it explains. As shown in drawing 34at the time of fast reproductionregenerative data is reproduced intermittently. The reproduced data is begun first and C1 decoding is given in the 1st error correction decoding circuit 25 according to the decoding algorithm shown in drawing 14.
[0077]On the other handin the ID detection circuit 24while detecting an ID signal based on the detection result of the synchronized signal outputted from the signal detection circuit 22the error in an ID signal is detected using the error detecting code added into the ID signal. And 1 error correction block which separates the above-mentioned data for special reproduction using the detected ID signaland is shown in drawing 7 is constituted. Specifically based on the track number to which the writing address to the memory 40 is added by the ID signaland a sink block (C1 block) numberit generates.
[0078]When an error correction is performed to the data in which the error correcting code was added in the different direction of [more than the 2-way which generally includes a recording direction as shown in drawing 7]When performing the error correction of a different direction from a recording directiononce memorizing the data of 1 error correction block to storage cellssuch as a memoryit is necessary to change the read-out direction of data and to perform an error correction. When an error is detected by the ID signal at that timethe data (in explanation of an error correctionone sink block is hereafter described as C1 block.) which is C1 block does not write data in the memory 40 in the 3rd error correction decoding circuit 28. When this compounds the data reproduced intermittently and it constitutes 1 error correction blockthe continuity of the ID signal is not guaranteed to be ordinary reproduction in things. When it seems that an address is presumed and the above-mentioned C1 block data in which the error was detected is generated using front C1 block ID information in the above-mentioned ID signalfor example as having no ID error in a pre-scanning periodIt is for the case where overwrite the data written in in the memory 40 and mistaken data is written in in the memory 40 to occur.
[0079]C4 decoding is given based on the decoding algorithm which shows drawing 15 1 error correction block shown in drawing 7 which comprised the above-mentioned point in the memory 40. The error detection flag from which an error correction and the detected data were detected with C4 or C1 check code by C4 check code is addedand the effective digital video signal except an error correcting code is read from the memory 40.
[0080]Since the writing to the memory 40 is controlled as mentioned above at the time of fast reproductionthe data by which error detection was carried out with the error detecting code in an ID signal is not written in the memory 40. Thereforewhen 1 error correction block is constitutedC1 block which the error

was detected and was not written in in the memory 40 into the ID signal occurs. At this timethe data in which the error correction rewritten by last time or second from last time was performed is memorized in the address which memorizes the above-mentioned C1 block in the memory 40. As a result of performing the error correction by C1 check code although all the data in C 1 block had mistaken itsince above-mentioned C1 block data was not updated when performing an error correction to this error correction blockit is judged that he has no error. Since the error detection flag with C1 numerals is resetthis is generated. Since the error correction is performed at the time of last time or the error correction before last even if it gives C1 decoding again to the C1 block data which is memorized in the memory 40 and which is not rewritten as for the account of the upperan error is undetectable. When this C1 block data performs the error correction by C4 check codeit serves as an overlooking error by C1 check code. (Especially when performing control which writes in C1 block data based on the above-mentioned ID information in the memory 40and performs C1 decoding to the written-in C1 block datathis phenomenon appears notably.)

[0081]As mentioned abovewhen performing the error correction by C4 check code in the state where the overlooking error by C1 check code is includedthe influence which the overlooking error (erroneous correction is included.) not only by the maximum exertion of the error correction capability by C4 check code not being carried out but C4 decoding increasesand it has on reproduction image quality is also great. Since high efficiency coding is given to the video signal at the time of record in the case of the home digital video tape recorder as shown especially in ****the overlooking error of one symbol will spread to the data of two or more above-mentioned DCT blocksand will degrade image quality. Thereforeit is necessary to correct or detect the error in regenerative data certainly.

[0082]In consideration of the above thingthe decoding algorithm of the error correcting code of this example 1 is shown in drawing 16 and drawing 17. The algorithm at the time of setting the data update flag of this example 1 was shown in drawing 16. The recording direction of this example 1 showed drawing 17 the error correction decoding (C4 decoding) algorithm using the error correcting code of a different direction (this example 1 perpendicular direction). C1 decoding algorithm is taken as what is shown in above-mentioned drawing 14and the same thing.

[0083]Hereafterthe error correction decoding algorithm of this example 1 is explained using drawing 16 and drawing 17. It begins first and the algorithm of the data update flag of this example 1 is explained using drawing 16. As for the C1 block data reproduced more nearly intermittently than the rotary head 19an ID signal is separated at first first. Error detection is performed using the error detecting code with which the separated ID signal is beforehand added at the time of record. After 1st 25Cerror correction decoding circuit 1 decoding is giventhe C1 block data judged that there is no error into an ID signal as a result of error detectionThe data area for special reproduction is separated based on the track number separated from the ID signaland a line numberand it is written in the

predetermined address in the memory 40. When writing above-mentioned C1 block data in the memory 40a data update flag is written in the predetermined address (address separated from the ID signal) of the renewal flag memory 41 of data. In this example 10shall be written in the renewal flag memory 41 of data as data update information about updated C1 block (refer to drawing 16). the renewal flag memory 41 of data -- decoding of 1 error correction block -- ending (C1 decoding and C4 decoding) -- the data update information in a memory is reset and all become non-update information. (That is1is altogether written in in a memory.)
[0084]The C1 block data judged to have no error in the ID signal in the ID detection circuit 24 is the 1st error correction decoding circuit 25and C1 decoding is given based on C1 decoding algorithm shown in drawing 14. (Since C1 decoding operation is the same as above-mentioned operationexplanation is omitted.) The data in which it is the above-mentioned point and C1 decoding was given is inputted into the 3rd error correction decoding circuit 28. Based on the error detection result of the ID signal outputted from the ID detection circuit 24the writing to the memory 40 of above-mentioned C1 block data is controlled by the 3rd error correction decoding circuit 28. Hereafterthe control method of the memory 40 and the renewal flag memory 41 of data is explained briefly. The ID signal detected in the ID detection circuit 24 and an error detection result are inputted into the error correction control circuit 44. As opposed to the data which is C1 block from which an error was not detected in the ID signal in the error correction control circuit 44The above-mentioned C1 block data to the memory 40 and the renewal flag memory 41 of datathe writing control signal of a data update flagand a writing timing signal are generated based on the track number information added to the ID signaland sink block number information. the above-mentioned writing timing signal whichin additiongenerated the control signal of the renewal flag memory 41 of data in the above-mentioned error correction control circuit 44. And it shall generate based on ID information in the update flag memory control circuit 42. In the memory 40above-mentioned C1 block data is written in the predetermined address in the memory 40 using the above-mentioned information detected from the ID signal. Similarlya data update flag (as mentioned above "0") is memorized by the renewal flag memory 41 of data. It memorizes to the predetermined address in C1 error-detection flag storage memory 53 which the error detection flag detected at the time of C1 decoding also mentions later.
[0085]On the other handthe C1 block data in which the error was detected in the ID signal is not written in in the memory 40but is canceled as it is. Thereforethe set of the flag to the renewal flag memory 41 of data and the above-mentioned C1 error-detection flag storage memory 53 is not performedeither. An error detection flag is memorized to an address predetermined [in C1 error-detection flag storage memory 53 in the error correction circuit 43] in the error detection flag with which the above-mentioned ID information points to the data in which the error was detected as a result of C1 decoding. In this example 1the data in which the error was detected at the time of C1 decoding shall also be written in the memory 40.

[0086]If the data of 1 error correction block in which C1 decoding was given in the above-mentioned way is compounded by the memory 40in the error correction control circuit 44the read-out start signal of a data update flag will be outputted to the update flag memory control circuit 42. Hereafterin the update flag memory control circuit 42an input of the above-mentioned data update flag read-out control signal will read data one by one from the data of the head of the renewal flag memory 41 of data. About the above-mentioned data update flag read from the renewal flag memory 41 of datait memorizes in the compulsive IREJA flag storage memory 52. In that casethe above-mentioned number of non-update flags (compulsive IREJA flag number) counts. The error detection flag number by C1 check code shall also be counted at the time of C1 decoding. In order to distinguish from the IREJA flag which shows hereafter the error detected by the C1 above-mentioned check code in above-mentioned C1 block non-update flag informationit is described as a compulsive IREJA flag for convenience.
[0087]Drawing 18 is an explanatory view of operation for explaining C4 decoding algorithm of the digital video tape recorder which is one example of this inventionand explains the count method of the above-mentioned number of IREJA taking the case of the error correction block shown in drawing 18. In the case of the example shown in drawing 18 (b) and (c)2 blocks and 3 blocks of compulsive IREJA will existandas for the error detected by C1 decodinga total of 5 blocks counts them as an IREJA flag number. About the case where the error detection flag is set by C1 block to which the compulsive IREJA flag is setthe number of IREJA is counted as that from which the error was detected at 1 C1 block.
[0088]Nextthe above-mentioned IREJA flag number is compared with the predetermined number n (this example 1 n= 6)andin more than n (in this example 1like a conventional exampleIREJA correction by C4 decoding shall be performed to the limit of the error correction capability which C4 check code hasand.)it is. IREJA correction shall be performed to 5 IREJA. In more than RC4 decoding is not performedcomparing the above-mentioned number of compulsion IREJA with the predetermined number R (this example 1 R= 6)but error correction operation is ended.
[0089]Since all the data in C 1 block on which this stands as mentioned above as for a compulsive IREJA flag is errorsAs shown in drawing 15even if the above-mentioned IREJA flag is disregarded in the case of C4 decoding and it performs an error correctionan error correction cannot be performed about the number of compulsive IREJA beyond the error correction capability (correction is possible to 2 errors) which C4 check code has. Since an error detection flag is added to all the blocks when an error correction is performed using C4 check code by forceit will not only be outputted as an error also about the data by which the error correction was carried out by C1 decodingbut the probability which causes erroneous correction becomes high. Thereforein this example 1when the number of compulsive IREJA is more than Rerror correction operation is terminated compulsorily.
[0090]On the other handwhen the number of compulsive IREJA flags is less than

R (the number of IREJA flags. more than n)C4 decoding is performed according to the algorithm shown in drawing 17. (In additionby this example 1as shown in drawing 17compulsive IREJA performs an error correction as disappearance.) Also when the number of IREJA is less than n similarlyas it is shown in drawing 17the error correction by C4 check code is performed. The details about the error correction by C4 check code are mentioned later.

[0091]After C4 decoding of 1 error correction block is completedthe update flag memory control circuit 42 resets the data update flag in the above-mentioned renewal flag memory 41 of data. Specificallyit goes "1" to the predetermined address in the renewal flag memory 41 of data to write in. An error detection flag is generated after the end of reset of the renewal flag memory 41 of data using the error detection flag by C1 check codethe error detection flag by C4 check codeand a compulsive IREJA flagand the error correction operation of 1 error correction block is ended. The reset timing of the above-mentioned renewal flag memory 41 of data and the timing of the set of an error detection flag are not restricted to above-mentioned timing. Reset of the above-mentioned C4 error-detection flag storage memory 54 in the error correction circuit 43C1 error-detection flag storage memory 53and the compulsive IREJA flag storage memory 52 shall be performed after an error detection flag set.

[0092]Operation of the reversion system at the time of the fast reproduction at the time of using drawing 16 and the decoding algorithm shown in drawing 17 based on the above thing is explained using drawing 1 - drawing 3drawing 16and drawing 17. As mentioned aboveif the mode signal of fast reproduction is inputtedthe switch 32 will choose the output of the switch 31. After the regenerative data intermittently reproduced via the rotary heads 20a and 20b is amplified with the head amplifier 21it is changed into reproduction digital data in the signal detection circuit 22and digital demodulation is performed in the digital demodulation circuit 23. Detection of a synchronized signal is also performed in the signal detection circuit 22. Data right and detected in the signal detection circuit 22 is inputted into the ID detection circuit 24 and the 1st error correction decoding circuit 25. In the ID detection circuit 24an ID signal is separated from a regenerative signal using the above-mentioned synchronized signaland the error contained in an ID signal using the error detecting code added into the ID signal is detected.

[0093]On the other handin the 1st error correction decoding circuit 25C1 decoding is performed based on the ID error information (existence of the error in an ID signal) outputted from the ID detection circuit 24. In this example 1C1 decoding shall not be performed about the C1 block (C1 block from which the error was detected in the ID signal) data in which the ID error was detected at the time of fast reproduction. (In this example 1C1 decoding is not performed about the C1 block data which detected the ID error at the time of fast reproduction.) As for thisthe C1 block cycle reproduced may become discontinuous in the case of a track jumpin order that two or more tracks may be crossed at the time of fast reproduction and it may reproduce dataand control may fail. In order to prevent

thisC1 decoding is stopped about the C1 block data which detected the ID error. If the protection circuit for not causing the above-mentioned breakdown is addedit cannot be overemphasized that C1 decoding may be given to the block which detected the ID error. C1 decoding is given based on the decoding algorithm shown in drawing 14 about the C1 block data in which an ID error was not detected. The data in which C1 decoding was given is inputted into the 3rd error correction decoder 28. As shown in ****C2 decoding is not performed at the time of fast reproduction.

[0094]Nextthe writing to the memory 40 of the C1 block data in which C1 decoding was givenand the writing of the data update flag 41 of a data update flag are briefly explained using drawing 16. The data which is C1 block from which the ID error was detected in the ID information detector circuit 24 is not written in the memory 40 as mentioned above. Thereforethe memory 40 and the renewal flag memory 41 of data will be in a waiting state until the following synchronized signal is detected.

[0095]On the other handif it is judged that he has no ID error in the ID information detector circuit 24in the update flag memory control circuit 42a data update flag will be set to the predetermined address of the renewal flag memory 41 of data based on an ID signal (a track number and C1 block number). (In this example 10is written in the renewal flag memory 41 of data.) Simultaneously with itthe C1 block data which generated the writing address to the memory 40 based on the ID signal and in which C1 decoding was given is written in the predetermined address in the memory 40 in the error correction control circuit 44. It repeats until the data of 1 error correction block which shows drawing 7 the above operation is compoundable. The error detected on the occasion of C1 decoding is written in the predetermined address in C1 error-detection flag storage memory 53 to which ID information points. In that casean error detection flag number with C1 numerals counts in the error correction circuit 43.

[0096]The data of 1 error correction block shown in drawing 7 is constituted in the memory 40and is not richat firstas mentioned abovefrom the renewal flag memory 41 of dataa data update flag is read and the compulsive IREJA flag storage memory 52 memorizes. A compulsive IREJA flag number counts in that case. After read-out of a data update flag is completedin the error correction core circuit 50the above-mentioned compulsion IREJA flag number and C1 error-detection flag number are addedand the number of IREJA is called for.

[0097]In the error correction core control circuit 51the decoding algorithm of C4 decoding is determined according to the above-mentioned number of IREJA. C4 decoding algorithm is explained using drawing 17. An input of the above-mentioned IREJA flag number will compare the above-mentioned IREJA flag number with the predetermined number n (n= 6) in the error correction core control circuit 51. And when the above-mentioned IREJA flag number is less than n (IREJA correction by C4 decoding shall be performed to the limit of the error correction capability which C4 check code hasand like a conventional example in this example 1.) IREJA correction shall be performed to 5 IREJA. IREJA correction is performed by

making the above-mentioned compulsion IREJA flag and C1 error-detection flag into IREJA. In that casethe overlooking error at the time of C1 decoding is performed to the limit of the error correction capability which C4 check code has.
[0098]Nextwhen the above-mentioned IREJA flag number is more than nin more than RC4 decoding is not performedcomparing the above-mentioned number of compulsion IREJA with the predetermined number R (this example 1 R= 6)but error correction operation is ended.
[0099]On the other handwhen the number of compulsive IREJA flags is less than R (the number of IREJA flags. more than n)in more than Pas compared with the predetermined number P (P= 4)only the above-mentioned compulsion IREJA flag is again made into IREJA for the number of compulsive IREJAand disappearance correction is performed. In that caseit overlooks at the time of C1 decodingand an error correction is not performed to an error. On the other handwhen the number of compulsive IREJA is less than PIREJA correction is performed by making only a compulsive IREJA flag into IREJA. In this casean error correction is performed to the limit of the error correction capability which is overlooked in the case of C1 decoding and C4 check code has also about an error.
[0100]On the other handin the error correction core control circuit 51an end of calculation of the number of IREJA will output a data request signal to the error correction control circuit 44. The error correction control circuit 44 will generate the read-out address of the data from the memory 40and a control signalif the above-mentioned data request signal is inputted. As for the data read from the memory 40syndrome is generated at first first in the error correction core circuit 50. After generation of syndrome is completedcorrection syndrome is generated based on a decoding algorithmand an error position and a numerical value are computed. After calculation of an error position and a numerical value is completedthe error correction core circuit 50 outputs the computed result of the above-mentioned error position to the error correction core control circuit 51. Since the case where it decodes using the Euclid algorithm in Example 1 is consideredalthough correction syndrome is searched forwhen it is other algorithmscorrection syndrome is not generated in the case of disappearance correctionbut it performs disappearance correction with syndrome and an elimination position.
[0101]The error correction core control circuit 51 will output error position data to the error correction control circuit 44 with an error data read-out request signalif the computed result of the above-mentioned error position is inputted. In the error correction control circuit 44the mistaken data memorized to the address to which error position data points is read from the memory 40. In the error correction core circuit 50an error correction is performed by adding the above-mentioned error numerical value to the mistaken data read from the memory 40. The data in which the error correction was performed is again written in the predetermined address to which the above-mentioned error position in the memory 40 points. The above operation is repeated by the detected error number. On the other handflag data is written in an address predetermined [in C4 error-detection flag storage memory

54] in the data in which the error was detected by C4 decoding. It is 1 error-correction-block ******** about the above-mentioned operation.
[0102]After C4 decoding of 1 error correction block is completedthe update flag memory control circuit 42 resets the renewal flag memory 41 of data in the above-mentioned way. The error detection flag after the end of reset of the renewal flag memory 41 of dataand by C1 check codeAn error detection flag is generated in the error detection flag generation circuit 56 using the error detection flag by C4 check codeand a compulsive IREJA flagthe generated error detection flag is memorized to the predetermined address of the error detection flag memory 57and the error correction operation of 1 error correction block is ended.
[0103]With the detected error detection flagthe data in which the error correction was performed in the above-mentioned way in the 3rd error correction decoding circuit 28 is read from the memory 40and is memorized to the 4th memory 29. By the 4th memory 29reproduction of all the data for special reproduction of one frame will output a data output requirement signal to the still picture packet generating circuit 30.
[0104]In this example 1at the time of fast reproductionif the special reproduction data for one above-mentioned frame (intra coding is carried out) is reproducedit will output from the 4th memory 29And in order to make a screen freeze by the ATV decoder side like still playback until the data for special reproduction for one following frame is reproduced (stillness)a still picture packet and a no data packet are generated in the still picture packet generating circuit 30. Data can be decoded without an ATV decoder being conscious of high speed reproduction mode like the time of still playback by the above-mentioned control. Hereafterthe data control method at the time of the above-mentioned fast reproduction is explained focusing on operation of the still picture packet generating circuit 30.
[0105]In the still picture packet generating circuit 30if a data output requirement signal is inputted from the 4th memory 29the situation of the still picture packet under present generating will be checked. Hereafteroperation is explained using drawing 19. Drawing 19 is a timing chart of the special reproduction of the digital video tape recorder which is one example of this invention. (a) in a figure The input signal of the 4th memory 29 (reproduced intermittently still in practice.)The data output requirement signal with which (b) is outputted from the 4th memory 29the data read-out start signal with which (c) is outputted from the still picture packet generating circuit 30As for the switching signal of the switch 31and (e)the output signal of the 4th memory 29 and (f) of (d) are the output signals of the still picture packet generating circuit 30.
[0106]When it begins first and the still picture packet is generated in the still picture packet generating circuit 30the 4th memory 29 will be in a waiting state until the output of the packet for one frame is completed (see the A points among a figure). And if the final packet of one frame of the still picture packet under above-mentioned output is outputtedthe still picture packet generating circuit 30 will output a data read-out start signal to the 4th memory 29. When the above-

mentioned no-data packet is generatedthe above-mentioned data read-out start signal is outputted after the completion of a packet output generated now (see the B points among a figure). By the 4th memory 29an input of the above-mentioned data read-out start signal will read the data packet for special reproduction in order from the inside of a memory.

[0107]On the other handconnection is switched so that the above-mentioned data read-out start signal may be supplied also to the switch 31 and the switch 31 may choose the output of the 4th memory 29. Switch-among figure 31 switching signal shall choose the output of the 4th memory 29 by "H"and shall choose the output of the still picture packet generating circuit 30 by "L." That the output of the 4th memory 29 will be in a waiting state when having generated the still picture packet as mentioned above in the still picture packet generation circuit 30It is because it is necessary to manage a reproduction frame in order to cause malfunction and to avoid thiswhen inter-frame data is disrupted on the way in an ATV decoder and intra-frame data is inputted.

[0108]If the final packet of the above-mentioned data for special reproduction is detected with the output of the 4th memory 29by the 4th memory 29the data output completion signal for special reproduction will be supplied to the still picture packet generating circuit 30 and the switch 31. With the switch 31an input of the above-mentioned signal will switch an output to the output of the still picture packet generating circuit 30. On the other handin the still picture packet generating circuit 30the packet outputted with the code amount by the present is switched. There is specifically too much data volume (frame number) transmitted to the ATV decoder sidewhen the memory in an ATV decoder is likely to cause overflowthe packet of no data is outputted and a code amount is controlled. It is too (underflow) few on the contraryor in being good exactlyit outputs the above-mentioned still picture packet. A still picture packet is the code quantity control (the memory in an ATV decoder as mentioned above) of an ATV bit stream by being outputted per frame and inserting the packet of no data between the above-mentioned still picture packets. [and] Or an output frame number is controlled not to cause underflow. It carries out. In this example 1the count of data volume (frame number) shall be counted in the output stage of the switch 32and shall output a counted result to the still picture packet generation circuit 30. Data volume is transmitted and is calculated by counting the number of sheets of the frame data by which a day code has not been carried out yetand its code amount. simple ---like -- the account of the upper -- the number of sheets of the frame data which has not been decoded yet may be sufficient.

[0109]As mentioned aboveby controlling the 4th memory 29the still picture packet generating circuit 30the switch 31and the switch 32a reproduced image can be constituted from an ATV decoderwithout being conscious of high speed reproduction modeand a good fast reproduction picture can be generated. By adopting combining the above-mentioned still picture packet and a no data packetoverflow of the memory in an ATV decoder and underflow can be preventedand a good special reproduction picture can be constituted.

[0110]Hereafterthe operation at the time of the mode transition of the still picture packet generating circuit 30 is explained. In the still picture packet generating circuit 30an input of a special reproduction mode signal will start generation of the above-mentioned still picture packet (a motion vector is 0 and a prediction error is a still picture packet of 0)and a no data packet. On the other handin the 3rd memory 27the final packet of the frame data in the ATV bit stream under present output is detected. And detection of the final packet of the above-mentioned frame data will supply the final packet detecting signal to the still picture packet generating circuit 30 and the switch 32. The switch 32 will be controlled to choose the output of the switch 31if the above-mentioned signal is inputted.
[0111]In the still picture packet generating circuit 30the above-mentioned final packet detecting signal is inputtedit does not begin not to be richthe still picture packet for one frame is generatedand a no data packet is generated following it. And the memory in an ATV decoder is kept from causing overflow or underflow by generating a no data packet in the still picture packet generating circuit 30. According to the output of the above-mentioned data volume which counted data volume in the output stage of the switch 32the number of insertion of the above-mentioned no-data packet shall be controlled by this example 1.
[0112]Drawing 20 is a timing chart at the time of shifting to special reproduction from the ordinary reproduction of the digital video tape recorder which is one example of this invention. In a figurea special reproduction mode signal and (c) show a frame final packet detecting signal(d) shows the switching signal of the switch 32andas for (a)(e) shows the output data of the still picture packet generating circuit 30as for the output of the 3rd memory 27and (b). As shown in a figurefrom the still picture packet generating circuit 30the above-mentioned still picture packet is outputted following the final packet of the frame of the data outputted from the 3rd memory 27. At this example 1change of a tape feed etc. shall also be performed to the same timing as the switching signal of the above-mentioned switch 32.
[0113]It can control by the above-mentioned operationwithout making an ATV decoder conscious of a state also about the time of the mode transition to special reproduction after the mode. Since the above-mentioned still picture packet is generated and outputted by this operation at the time of the mode transition to special reproductionthe reproduction screen at the time of mode transition can perform mode transition smoothlywithout becoming a still picture and disturbing a screen. Especially a digital video tape recorder that records the above-mentioned ATV signalEven if it uses the data reproduced at the time of mode transition unlike VTR of the conventional analog recordingan ATV signal as mentioned above Intra-frameAnd since it comprises an inter-frame bit stream and the regenerative signal reproduced from the rotary head 20 cannot constitute a special reproduction picturethe above control becomes very effective.
[0114]The switch 31 will choose the output of the still picture packet generation circuit 30if the above-mentioned special reproduction mode signal is inputted. The switching control of the switch 31 controls a graphic display to choose the output

of the still picture packet generation circuit 30 until it shifts to special reproduction mode and a tape travel system (servo system) locks (stationary state)although not carried out. If a tape travel system goes into a stationary state and the above-mentioned data for special reproduction for one frame is compounded within the 4th memory 29a data output requirement signal will be outputted as mentioned above than the 4th memory 29. Since control of the subsequent still picture packet generating circuits 30the switch 31the switch 32and the 4th memory 29 is the same as that of the items mentioned at the time of the above-mentioned fast reproductionexplanation is omitted. (Refer to drawing 19)

[0115]Nextthe control method at the time of shifting to ordinary reproduction mode from special reproduction mode is explained. If an ordinary reproduction mode signal is inputted when shifting to ordinary reproduction mode from special reproduction modethe 4th memory 29 will check the output situation of the present data. While outputting a data output completion signal to the still picture packet generating circuit 30 after reading the data for one framewhen the data packet for the above-mentioned special reproduction is read from the 4th memory 29 nowthe writing of the data to the 4th memory 29 is stopped. An ordinary reproduction mode start signal is outputted to a tape travel system (servo system) simultaneously with it. In the still picture packet generating circuit 30an input of the above-mentioned data read-out completion signal will generate and output a still picture packet and a no data packet so that the memory by the side of an ATV decoder may not cause overflow or underflow in the above-mentioned way. It is outputted to above-mentioned timing also about the switching control signal of the switch 31. (Refer to it A points of drawing 19)

[0116]When the data packet for the above-mentioned special reproduction is not read from the 4th memory 29the 4th memory 29 outputs an ordinary reproduction mode start signal to a tape travel system (servo system) while stopping the writing of data. In the still picture packet generating circuit 30a still picture packet and a no data packet are generated and outputted so that the memory by the side of an ATV decoder may not cause overflow or underflow like ****and as for the switch 31the output of the still picture packet generating circuit 30 is chosen. (Refer to it B points of drawing 17)

[0117]In a tape travel system (servo system)if an ordinary reproduction mode start signal is inputted from the 4th memory 29 of the aboveit will shift to ordinary reproduction mode. And if a tape travel system will be in a stationary stateit will output having become ordinary reproduction to the 3rd memory 27 and the 4th memory 29. If it becomes ordinary reproductionby the 3rd memory 27the reproduced ATV data for the above-mentioned ordinary reproduction will be written in in a memory. By the 4th memory 29the data for special reproduction is again written in in the 4th memory 29 in a similar manner.

[0118]The transport packet of ATV is constituted and the ATV data written in in the 3rd memory 27 is outputtedafter the data for special reproduction is removed by a memory. And in the latter part of the 3rd memory 27the switch 32 chooses

the output of the switch 31 until leading packets intra-frame in the beginning are detected first. If an intra-frame head is detected by the outgoing end of the 3rd memory 27a detection result will be supplied to the switch 32. With the switch 32an input of the above-mentioned signal will choose the output of the 3rd memory 27. While being able to perform mode transition smoothly and being able to obtain good reproduction image quality by the above-mentioned controlwithout confusing a reproduced image at the time of the shift to each mode signal from ordinary reproductionor shift of special reproduction mode to ordinary reproduction modeA reproduced image can be constituted without being conscious of mode transition about an ATV decoder.

[0119]The output of the switch 32 is outputted to an ATV decoder. Since the above-mentioned digital video tape recorder is controlled as mentioned above at the time of fast reproductionWhile the same control as ordinary reproduction can constitute a special reproduction picture from an ATV decoderwithout being conscious of the reproduction mode of a digital video tape recorderthe memory space of the 4th memory 29 used at the time of special reproduction is reducible. The 4th memory 29 does not need to repeat the same data in a memory two or more times by the above-mentioned controland this does not need to read itas shown in drawing 19 (f). This shows that the memory has openedafter reading data once. Thereforefast reproduction is realizable only by adding a buffer memory to the preceding paragraph of the 4th memory 29. When the above-mentioned control was not performedneeded to read the reproduced data for special reproduction repeatedly until the following data for special reproduction was reproducedneeded the memory for the special reproduction for at least two framesand were not able to aim at reduction of memory spacebut. The composition of this example 1 can realize special reproduction by the memory for about one frame as mentioned aboveand memory space can be mostly made into a half.

[0120]It is not what it constituted from this example 1 so that it might outputonce it memorized data of one frame in the 4th memory 29but is restricted to thisThe data written in the 4th memory 29 per plural slices as shown in drawing 21 is readThe above-mentioned no-data packet is outputted as a packet during the slice in the same frameand in inter-frameeven if it switches and outputs the above-mentioned still picture packet and a no data packetthe same effect is done so. Drawing 21 shows the case where one frame outputs the data divided into two or more slices to an ATV decoder in plural-slices collection n step (the special reproduction picture of one frame is divided into n blocks by making a slice into a unit.). n is two or more integers. The number of slices contained in n above-mentioned blocks does not need to be the same. Reduction of the memory space of the 4th memory 29 can be aimed at by above-mentioned composition.

[0121]In this example 1it overflows beforehand to an ATV decoder in the still picture packet generating circuit 30And it is not what the still picture packet and the no data packet were combined beforehandand control of the code amount and the frame number was performed so that underflow might not be causedbut is restricted to thisEspecially about a no data packetthe packet indicating the modes

other than a video signalfor examplethe packet etc. to which the header information indicating an audio signal is addedmay be inserted. In this caseif a packet which becomes result predetermined DC data of voice decoding is generated and outputted in order to perform audio mute by an ATV decodervoice mute is also made and good special reproduction can be realized.

[0122]Although the above-mentioned Example 1 explained the control method of the 3rd memory 27 of the above at the time of the mode transition at the time of fast reproductionthe 4th memory 29the still picture packet generating circuit 30the switch 31and the switch 32The above-mentioned control method is not restricted to fast reproductionand from the mode transition to the above-mentioned still playback or the mode transition from still playback to ordinary reproductionand fast reproductioneven if it uses slow reproductionreversely [its]etc. from still playback or its contraryand ordinary reproductionit does the same effect so. Although reference was not made about slow reproduction in this example 1Since slow reproduction is realizable by repetition of still playbackit cannot be overemphasized by using it as mentioned aboveswitching regenerative data and a still picture packet (a no data packet is included.) that it is realizable like Example 1.

[0123]It is not what is restricted to this although the digital video tape recorder which records the ATV signal currently deliberated in the U.S. in this example 1 was describedFor examplethe above-mentioned still picture packet and a no data packet may be used for the control at the time of the special reproduction of a digital video tape recorder which records the bit stream of MPEG 2. The recording and reproducing device of the above-mentioned signal is not what is restricted to a digital video tape recorderFor examplethe same effect is done soeven if it uses for a case so that a reproduced image may be constituted only using the data by which intra coding was carried out in the ATV bit stream or the bit stream of MPEG at the time of special reproductionsuch as reproduction or a disk unit which carries out record reproduction.

[0124]It is not what the decoding algorithm shown in drawing 17 by this example 1 was used when decoding C4 decodingbut is restricted to thisIf it is a decoding algorithm using the above-mentioned compulsion IREJA flagwhen decoding the error correction block which adopts product-code form like the C2 above-mentioned numerals or C3 numeralseven if it usesan error correction can be performed effectively and the same effect is done so. When decoding the block coded more than the duplexeven if it uses and decodes the above-mentioned compulsion IREJA flagit cannot be overemphasized that an error correction can be performed effectively.

[0125]In above-mentioned Example 1although the case where the above-mentioned compulsion IREJA flag is used at the time of fast reproduction is explainedit does not restrict to thisand when performing an error correction to regenerative data for exampleat the time of slow reproductioneven if it usesthe same effect is done so. The same effect is done so even if it uses the above-mentioned compulsion IREJA flag at the time of ordinary reproduction. (Especially

when a long dropout occursit can decode effectively.)
[0126]Although controlled by the error detection result of the ID information to which the writing to the memory 40 is added by the ID signalit does not restrict to this. For exampleit cannot be overemphasized that C1 decoding result etc. may be used.
[0127]Switching control of the above-mentioned threshold level nRand P may be carried out for the decoding algorithm shown in above-mentioned drawing 17 in each mode of ordinary reproduction and special reproduction. The number of the maximum IREJA corrections may be small set up compared with ordinary reproduction so that especially data may stop an overlooking error with C4 numerals in the fast reproduction reproduced intermittently or slow reproduction. (For exampleit is set as n= 5R= 5and P= 3 to n= 6R= 6and P= 4 at the time of fast reproduction at the time of ordinary reproduction)
[0128]It is not what is restricted to the algorithm shown in drawing 17 about C4 decoding algorithmIf it controls to treat the above-mentioned compulsion IREJA flag as IREJAand to switch the algorithm of C4 decoding with a compulsive IREJA flag numberthe error correction which uses for the maximum the error correction capability which C4 numerals have is realizable.
[0129]At this example 1it cannot be overemphasized that the renewal flag memory 41 of data and the compulsive IREJA flag storage memory 52 are separatedand operation is explained in order to explain simplybut it may not restrict to thisand may use in common. It is not what is restricted to this although decoded by distinguishing the above-mentioned compulsion IREJA flag and C1 error-detection flag in this example 1It can decode by utilizing the error correction capability of an error correcting code enough as compared with the case where a compulsive IREJA flag is not used even if the two above-mentioned flags are not distinguished but it decodes. ****** -- in that casethe above-mentioned compulsion IREJA flag storage memory 52 and C1 error-correction flag storage memory may be shared.
[0130]It is not what is restricted to this although the data in which the error was detected in this example 1 as a result of C1 decoding was written in the memory 40 (or memory in the 2nd error correction decoding circuit)The same effect is done so even if it controls not to write in the data which is C1 block from which the error was detected as a result of C1 decoding in the memory 40. (In additionthe above-mentioned compulsion IREJA flag and C1 error-detection flag shall not be distinguished as mentioned above in this casebut it shall control) AgainThe same effect is done soeven if it constitutes from this example 1 so that C1 decoding and C4 decoding (it is C2 decoding at the time of ordinary reproduction) may be given once not restricting to this and storing regenerative data in a memoryalthough the data which performed C1 decoding was considered as the composition written in a memory.
[0131]It is not what is restricted to this although the error correction was performed in above-mentioned Example 1 to the limit of the error correction capability which C4 numerals have at the time of an error correction with C4 numeralsWhen there are many above-mentioned compulsion IREJA flagsin order to

improve error detecting capabilityit cannot be overemphasized that it may control to set up an error correction or the number of IREJA corrections fewand to improve error detecting capability.

[0132]As the above-mentioned Example 1 shows to drawing 7as numerals of a recording direction the Reed Solomon code of (85779)The same effect will be done soif it does not restrict to this and decodes also with the error correcting code of other product-code forms using the above-mentioned compulsion IREJA flagalthough the case where the Reed Solomon code of (20156) was adopted as vertical numerals was explained.

[0133]When error correction decoding is repeatedly performed using the error correcting code of the above-mentioned recording direction (with repetition error correction decoding.) It constitutes so that the error correction capability of the recording direction at the time of decoding repeatedly by the existence of the decoding method and the above-mentioned update flag which use C1 numerals for the data in which gave C4 decoding after giving C1 decodingand C4 decoding was given furtherand perform an error correction again may be switched. As mentioned abovesince a decoding algorithm is switched by the existence of an update flagespecially about above-mentioned renewal Cof sheep 1 block datathe overlooking error in the case of decoding can be stopped repeatedlyand a good reproduced image can be compounded.

[0134]When error correction decoding is repeatedly performed using the error correcting code of the above-mentioned recording directionWhen the above-mentioned update flag decodes the reproduction digital data in a reset state (data which is renewal Cof un-1 block)Since the disappearance correction using the error detection flag detected with the error correcting code (C4 numerals) of a different direction from the above-mentioned recording direction is controlled not to carry outEspecially about above-mentioned renewal Cof sheep 1 block datathe overlooking error in the case of decoding can be stopped repeatedlyand a good reproduced image can be compounded.

[0135]It is not what is restricted to this although the above-mentioned Example 1 described the case of the Reed Solomon code which is a linearity error correcting codeFor examplealso when an error correcting code is constituted from a BCH code or a BCH codeand an above-mentioned Reed Solomon codethe same effect is done so by using the above-mentioned compulsion IREJA flagwhen performing IREJA correction.

[0136]In this example 1although the decoding algorithm of an error correcting code which used the above-mentioned compulsion IREJA flag about reproduction of the video signal is explainedit does not restrict to thisand the effect that an audio signal is also the same is done so. Although the above-mentioned Example 1 explained taking the case of the case of a digital video tape recorderdo not restrict to this and DATIf it is CDa mini discand digital signal playback equipment that plays the digital signal represented by the disk recorder of digital recordingit cannot be overemphasized that the same effect is done so.

[0137]When adding an error detection flag in the error correction circuit which

adopts the decoding algorithm using the above-mentioned compulsion IREJA flagA compulsive IREJA flag number performs an error correction as IREJA only a compulsive IREJA flag with less than a predetermined number (for example3) (in the case of drawing 17the number of IREJA is six or more)The total number of IREJA about the data of few error correction blocks from a predetermined number (for example9) C1 error-detection flagor the data which stands as for both the compulsive IREJA flag and the above-mentioned C4 error-detection flag is made into an error (A amendment)and an error detection flag is added for all the errors detected with C4 numerals as an error about the data of error correction blocks other than the above -- it controls like (B amendment). When adding an error detection flag by the above compositionwhile being able to add an error detection flag certainly and being able to stop an overlooking error as much as possiblean error detection flag number can also be stopped enough.

[0138]It is not what the memory which memorizes the above-mentioned IREJA flag was separately provided as shown in drawing 2 and drawing 3but is restricted to thisFor examplewhen it constitutes the above-mentioned memory 40 using a commercial memory and 1 error correction block of above-mentioned drawing 7 is constitutedempty area occurs in the memory 40. The above-mentioned error detection flag or a data update flag may also be written in the area. Since it is most to comprise 8 bitsthe memory of marketing used for the above-mentioned error correction may be constituted so that the above-mentioned data update flag and C1 error-detection flag may be memorized in the bit from which the same address differs. Since the above-mentioned data update flag (compulsive IREJA flag) and C1 error-detection flag can be read at once in the case of C4 decoding if constituted as mentioned abovereduction of circuit structure can be aimed at.

[0139]The reset timing of the flag data in the renewal flag memory 41 of datathe compulsive IREJA flag storage memory 52C1 error-detection flag storage memory 53and C4 error-detection flag storage memory 54 is not restricted to the above-mentioned timing. For examplethe renewal flag memory 41 of data may reset datareading flag data at the time of C4 decoding. (Rendering)

[0140]Example 2. drawing 22 is a block lineblock diagram of the reversion system of the digital video tape recorder which is one example of this invention. In a figuredrawing 1 and identical parts ** identical codesand since the composition and operation are the same as that of drawing 1explanation is omitted. 34 is a header attachment **** circuit which attaches and changes the inputted header of a transport packet. The recording format of the digital video tape recorder in this example 2 presupposes that it is the same as that of the above-mentioned Example 1.

[0141]This example 2 records an ATV bit stream in an above-mentioned way (the data for special reproduction from a bit stream specifically). [separate and] The capacity of the memory used in the digital video tape recorder which records the data for special reproduction which dissociated [above-mentioned] on the area where the recording track was defined beforehand at the time of fast reproduction is reduced.

[0142]Hereafteroperation of the reversion system at the time of the fast reproduction of the digital video tape recorder in this example 2 is explained using drawing 22. This example 2 explains the case of the composition of the rotary head shown in drawing 5 (a) like Example 1. The scanning locus of the rotary head 20a at the time of performing twice4 times8 timesand 16X reproduction becomes like drawing 12 like Example 1. The tracking of the rotary head 20 (a) shall be controlled so that a reproducing output becomes the maximum at the center of area that the above-mentioned data for special reproduction is recorded in each double-speed number about the tracking control method at the time of fast reproduction as well as Example 1. (Refer to drawing 13 (a) - (c))

[0143]Based on the above thingoperation of the reversion system at the time of fast reproduction is explained using drawing 22drawing 12and drawing 13. If the mode signal of fast reproduction is inputtedthe switch 32 will choose the output of the switch 31. (About the timing that in addition a switch-off substitute is fineit is considered as the same timing as Example 1.) The rotary head 20aAnd after the regenerative data intermittently reproduced via 20b is amplified with the head amplifier 21it is changed into reproduction digital data in the signal detection circuit 22and digital demodulation is performed in the digital demodulation circuit 23. Data right and detected in the signal detection circuit 22 is inputted into the ID detection circuit 24 and the 1st error correction decoding circuit 25. In the ID detection circuit 24the ID signal added to the head part of each sink block on the basis of the synchronized signal detected in the signal detection circuit 22 is separatedand the error contained in an ID signal using the error detecting code added into the ID signal is detected.

[0144]On the other handin the 1st error correction decoding circuit 25correction of the error which was with C1 check code added to the recording directionand was generated in the regenerative signaland detection are performed. The data in which C1 decoding was given is inputted into the 3rd error correction decoder 28. The output of the 1st error correction decoding circuit 25Although inputted also into the 2nd error correction decoding circuit 26since data is reproduced intermittently as mentioned aboveC2 decoding cannot be performed and a transport packet cannot be generatedin this example 2C2 decoding operation shall not be performed like Example 1 at the time of fast reproduction.

[0145]As for the data for special reproduction in which 2nd 25Cerror correction decoding circuit 1 decoding was given3rd 28Cerror correction decoding circuit 4 decoding is given. Since it is the same as that of Example 1 also about C4 decoding operationdetailed explanation is omitted. The data in which 3rd 28Cerror correction decoding circuit 4 decoding was given is memorized by the 4th memory 29.

[0146]When the bit stream represented with this example 2 by MPEG 2 is recorded on a digital video tape recorderin order to realize special reproductionthe Intra picture is extracted from the above-mentioned bit streamand the above-mentioned intra-frame data is recorded on the data recording area for special reproduction beforehand provided all over the recording track. In that casethe

capacity of the memory used at the time of fast reproduction is reduced.
[0147]Hereafteroperation of the 4th memory 29 of the above at the time of the fast reproduction of a forward directionthe still picture packet generating circuit 30the switch 31and the header attachment **** circuit 34 is explained using drawing 21. Usuallyin order to transmit the data by which intra coding was carried out at the time of special reproduction per framethe memory which memorizes data of one frame as shown in Example 1 as a memory for special reproduction is required. In this example 2as shown in drawing 21one or more slices are collected by the 4th memory 29and the Intra picture of one frame is divided into n blocksand is outputted (it is hereafter described as a slice block.). Per slicethe data for special reproduction counts the code amount reproducedand constitutes a slice block from the 4th memory 29. In this example 2a slice block is constituted from a place where the code amount of the data for special reproduction memorized by the 4th memory 29 became a predetermined valueand data is read from the 4th memory 29.
[0148]After the output of the data of the above-mentioned 1 slice block is completedthe 4th memory 29 outputs a data output requirement signal to the still picture packet generating circuit 30. outputting the above-mentioned no-data packet as a packet during the above-mentioned slice block in the same frame in the still picture packet generating circuit 30 -- inter-frame -- the above-mentioned still picture packet and a no data packet -- a predetermined frame number output -- it carries out. In this example 2it transmits as INTAFUREMUMODO (mode of between the fields or inter frame prediction) as output mode of a transport packet. In this casethe data for special reproduction of the slice unit intermittently reproduced at the time of fast reproduction is controlled to transmit as the compulsory intra-frame mode. Drawing 21 shows the case where one frame is divided into n slice blocks. (n is two or more integers)
[0149]Hereafterthe data control method at the time of the fast reproduction of above-mentioned this example 2 is explained focusing on operation of the still picture packet generating circuit 30 and the header attachment **** circuit 34. In this example 2as a transport packeteven if the data for special reproduction is treated as an intra-frame picture and it transmits itit does the same effect so.
[0150]As mentioned abovein this example 2the transport packet to output is transmitted as a packet of INTAFUREMUMODO at the time of the fast reproduction of a forward direction. In order to freeze a screen by the ATV decoder side at the time of special reproduction (stillness)a still picture packet and a no data packet are generated between the data packets for special reproduction of one frame in the still picture packet generating circuit 30 (refer to drawing 21). Therebyin an ATV decodera good fast reproduction picture can be outputted like Example 1without being conscious of special reproduction mode. Hereafterthe operation after the 4th memory 29 is explained using drawing 22.
[0151]Afteras for the data for special reproduction reproduced via the rotary head 20digital demodulationan error correctionetc. are performedthe 4th memory 29 once memorizes and a slice is constituted. The slice which comprised the 4th

memory 29 is outputted to the header attachment **** circuit 34 via the switch 31. While attaching to the header which detects the header part indicating the transmission mode of the picture in a packet header (MPEG 2 picture header) in the header attachment **** circuit 34and points to inter-frame (or INTAFIRUDO) one and changingit is a macro block (in addition). At MPEG 2the decoding mode of a block is switched by a macro block unit. The header unit indicating decoding mode is detectedand this header is attached to the header of the Intra frame modeand is changed. The data packet for special reproduction for which the header was changed is supplied to the output terminal 33 via the switch 32. while the transport packet which transmits the data for special reproduction is transmitted as an inter-frame packet by this -- the data of each macro block -- compulsion -- intra -- it is decoded by an ATV decoder as that of a frame mode.

[0152]On the other handan end of the output of the transport packet for the special reproduction for one frame will output a still picture packet from the still picture packet generating circuit 30. Similarlywith the switch 31an end of the output of the transport packet for the special reproduction for one above-mentioned frame will choose the output of the still picture packet generating circuit 30. (In additiongenerating timing of a still picture packet and switching timing of the switch 31 are taken as the same thing as Example 1.) The output (still picture packet) of the switch 31 is supplied to the switch 32 via the header attachment **** circuit 34. It shall generate all over the still picture packet generating circuit 30and a header shall attach the header part of a still picture packet by this example 2 in the header attachment **** circuit 34and it shall not perform ****.

[0153]In this example 2since an output transport packet is controlled as mentioned abovethe memory space of the 4th memory 29 is substantially reducible compared with the case of Example 1. As shown in Example 1 that what is necessary is just to arrange the memory which can specifically memorize the data for one slice (it is a part for a number slice depending on the composition of a slice)it is not necessary to arrange the memory for one frame to the reversion system side. In particularin a reproduction special-purpose machinesince it is not necessary to have a memory for one framereduction of circuit structure can be performed. A transport packet can be decoded without carrying out special reproduction mode consciousness about an ATV decoder.

[0154]Example 3. this example 3 explains the transmission method of other data. Once transmitting the data for special reproduction for one frame to an ATV decoderthe above-mentioned transmission method was constituted so that a part for a predetermined frame number and the above-mentioned still picture packet might be generated and transmitted in the still picture packet generating circuit 30. This example 3 explains the case where divide the above-mentioned special reproduction data into two or more framesand it is transmitted. Let composition of the reversion system of a digital video tape recorder in this example 3 be the same thing as what is shown in drawing 22.

[0155]Drawing 23 is a figure for explaining the state of the regenerative data at

the time of the special reproduction for Masakata of the digital video tape recorder which is one example of this inventionand drawing 26 is a figure for explaining the state of the regenerative data at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this invention. Compound the data for special reproduction intermittently reproduced at the time of fast reproductionand the above-mentioned slice block is constituted from this example 3The transport packet of one frame is generated combining the still picture packet generated in this slice block and the above-mentioned still picture packet generating circuit 30and it outputs to an ATV decoder. (It is hereafter described as a partial refreshing system.)

[0156]Hereafterthe above-mentioned partial refreshing system at the time of performing fast reproduction of a forward direction is explained using drawing 23 and drawing 24. When fast reproduction of a forward direction is performed to drawing 23 (a)the data for special reproduction reproduced from the rotary head 20 is shown. (In practiceit is reproduced intermittently.) The output transport packet outputted to the figure (b) from the switch 32 is shown. The transport packet for one frame is shown in one frame described into the figure. The switching signal of the switch 31 is shown in the figure (c). Drawing 24 is a figure showing the partial refreshment on the screen at the time of the special reproduction for Masakata of the digital video tape recorder which is one example of this invention. The data for special reproduction in which the data of the portion which gave the slash is compulsorily transmitted by an intra mode is shown among a figureand other portions show the transmission parts of the still picture packet outputted from the still picture packet generating circuit 30. In this example 3as shown in drawing 23the picture for special reproduction of one frame is divided into n slice blocksand is transmitted.

[0157]Hereafteroperation of the reversion system at the time of the fast reproduction of a forward direction is explained using drawing 22drawing 23and drawing 24. Since the operation to the 3rd error correction decoding circuit 28 is the same as that of Example 2explanation is omitted. The data for which regenerative-signal processing was performed as mentioned aboveand 3rd 28Cerror correction decoding circuit 4 decoding was given is memorized by the 4th memory 29.

[0158]In this example 3when the digital video tape recorder which adopts the above recording methods like Example 2 performs fast reproductionthe memory space of the memory for special reproduction (the 4th memory 29) used at the time of fast reproduction is reduced.

[0159]Hereafteroperation of the 4th memory 29 of the above at the time of the fast reproduction of a forward directionthe still picture packet generating circuit 30the switch 31and the header attachment **** circuit 34 is explained using drawing 22. Usuallyin order to perform data communications per frame by which intra coding was carried out at the time of special reproductionthe memory which memorizes data of one frame as shown in Example 1 as a memory for special

reproduction is required. As shown in drawing 23 or drawing 24collect two or more slices by the 4th memory 29and a slice block is constituted from this example 3The still picture packet outputted from the above-mentioned slice block and the still picture packet generating circuit 30 is combinedand the transport packet of one frame is constituted and outputted. The code amount of the data for special reproduction is counted per sliceand a slice block consists of the 4th memory 29. In this example 3a slice block consists of places where the code amount of the data for special reproduction memorized by the 4th memory 29 like Example 2 became a predetermined valueand data is read from the 4th memory 29.

[0160]After the composition of the data of the above-mentioned 1 slice block is completedthe 4th memory 29 outputs a data output requirement signal and the macro block address included in the above-mentioned slice block to the still picture packet generating circuit 30. By the standard of MPEG 2when transmitting a packetthe macro block of one frame is divided and transmitted to a slicebut it is defined as transmitting transmitting order in order of a raster scan from the macro block at the upper left of a screen top. Thereforein this example 3the address of the macro block of the head within a slice block and the last macro block address are transmitted as address information of a macro block. In the still picture packet generating circuit 30if the above-mentioned signal is receivedit will begin firstand the still picture packet to the macro block in front of [of a top macro block] one will be generated and outputted following the header information (MPEG 2 picture header) which puts and shows that it is inter-frame (field). When the data for special reproduction is a head of a framesince the above-mentioned header (MPEG 2 picture header) is added beforehandaddition is not performed. Under the present circumstancesthe switch 31 chooses the output of the still picture packet generating circuit 30. And after the output of the still picture packet to the macro block address of the above-mentioned head is completedthe still picture packet generating circuit 30 outputs a data read-out start signal to the 4th memory 29.

[0161]In the 4th memory 29if the above-mentioned signal is receivedthe slice block which constituted the point will be read from a head. Under the present circumstancesthe switch 31 chooses the output of the 4th memory 29. An end of read-out of the above-mentioned slice block will output the control signal which shows that read-out of data was completed to the still picture packet generating circuit 30. In the still picture packet generating circuit 30if the above-mentioned signal is receivedthe still picture packet to the last macro block of one frame will be generated and outputted from the next macro block of the last macro block of a slice block. In that casethe switch 31 chooses the output of the still picture packet generating circuit 30 again. If generation of the still picture packet to the last macro block of one frame is completedthe still picture packet generating circuit 30 shall output a no-data packet until the following composition of a slice block is completed.

[0162]On the other handthe output of the switch 31 is inputted into the header attachment **** circuit 34. In this example 3a transport packet is transmitted as INTAFUREMUMODO (mode of between the fields or inter frame prediction) like

Example 2. In this casethe data for special reproduction of the slice unit intermittently reproduced at the time of fast reproduction is controlled to transmit as the compulsory intra-frame mode. In the header attachment **** circuit 34. While attaching to the header which detects the header part indicating the transmission mode of the picture in a packet header (MPEG 2 picture header) about the data packet for special reproduction like Example 2 and to which it points inter-frame (or INTAFIRUDO) ones and changingThe header unit indicating the decoding mode of a macro block is detectedand this header is attached to the header of the Intra frame modeand is changed. The data packet for special reproduction for which the header was changed is supplied to the output terminal 33 via the switch 32. while the transport packet which transmits the data for special reproduction is transmitted as an inter-frame packet by this -- the data of each macro block -- compulsion -- intra -- it is decoded by an ATV decoder as a frame mode.

[0163]On the other handthe still picture packet outputted from the still picture packet generating circuit 30 is supplied to the switch 32 via the header attachment **** circuit 34. It shall generate all over the still picture packet generating circuit 30and a header shall attach the header part of a still picture packet like [in this example 3] Example 2 in the header attachment **** circuit 34and it shall not perform ****.

[0164]The timing chart in the case of dividing the data packet for special reproduction of one frame into the transport packet of the n frameand transmitting it to drawing 23 and drawing 24 and the situation of refreshment of the screen of frame data transmitted were shown. By transmitting dataas shown in the figurethe screen of one frame will be updated by plural slices for every frameand all the special reproduction pictures will be updated with the n frame (partial refreshment).

[0165]As mentioned abovein this example 3the transport packet to output is transmitted as a packet of INTAFUREMUMODO at the time of the fast reproduction of a forward direction. In order to freeze a screen by the ATV decoder side at the time of special reproduction (stillness)Since the screen information in one frame which is not refreshed generates a still picture packet and a no data packet in the still picture packet generating circuit 30 (refer to drawing 23)it can output a good fast reproduction picture like Example 1 in an ATV decoderwithout being conscious of special reproduction mode.

[0166]Nexthow to reduce the capacity of the 4th memory 29 at the time of the fast reproduction of an opposite direction is explained. In Example 2at the time of the fast reproduction of a forward directiontwo or more blocks reproduction slices were collected by the 4th memory 29and the data packet for special reproduction was outputted from the 4th memory 29 by the slice block unit which constituted and constituted the slice block. And by inserting a no data packet between the slice block in the same frameand a slice blockand inserting a still picture packet in each inter-frame onethe transport packet at the time of fast reproduction was generatedand this reduced the memory space of the memory for special reproduction. Since data is recorded in order of the slice into which a bit stream is

inputted for the above-mentioned data for special reproduction as for thisEven if a slice block is constituted as mentioned above and it outputs regenerative data by a slice block unitit is not necessary to replace the turn of the above-mentioned slice reproduced at the time of the fast reproduction of a forward direction. Thereforebefore constituting data of one framesubsequent data was able to be outputted per slice.

[0167]On the other handwhen the time of the fast reproduction of an opposite direction is performedthe above-mentioned slice is reproduced in turn opposite to the time of record. Howeverby the standard of MPEG 2the transmitting order of a macro block must transmit in order of a raster scan from the macro block arranged at the screen upper left as mentioned above. Thereforein an ATV decoderan input of intra-frame data will start decoding of image data from a top slice. When the transmitting order of the slice in an input bit stream differs from predetermined turn in that casea reproduced image cannot consist of ATV decoders. Since it is not supportedthe function in which this carries out the DESHAFU ring of the above-mentioned slice decoded to the position on a screen when the turn under slice reproduced [above-mentioned] differed in an ATV decoder (standard of MPEG 2) is produced. In such a caseif it is going to realize fast reproduction of an opposite directionit is necessary to prepare for a reversion system the memory which can memorize the above-mentioned data for special reproduction for at least one frameand to rearrange the reproduced data.

[0168]Drawing 25 is an explanatory view of operation at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this inventionand shows drawing 25 (a) the example of composition of the slice block in one frame. The scanning locus of the rotary head 20 at the time of performing -2X reproduction (a) is shown in the figure (b). The regenerative signal outputted to the figure (c) from the rotary head 20 (a) is shown. The data for special reproduction of one track shall constitute the above-mentioned slice block from this example. Since the data of a slice block is reproduced conversely as mentioned abovea transmission method (after outputting the data for special reproduction for one framepredetermined number transmission of the still picture packet is carried out.) as shown in Example 2 cannot be performed. Thereforeit is necessary to rearrange data by the 4th memory 29. In order to account[of the upper]-arrange at the time of the fast reproduction of an opposite directionto changeand not to need a memory hereafter but to decode a regenerative signal correctlythe data control method at the time of using the above-mentioned partial refreshing system by the fast reproduction of an opposite direction is explained.

[0169]Thereforethe transport packet outputted like the time of the fast reproduction of a forward direction is transmitted as a packet of INTAFUREMUMODO (mode of between the fields or inter frame prediction) also at the time of the fast reproduction of an opposite direction. In that casethe data for special reproduction intermittently reproduced at the time of the fast reproduction of an opposite direction is controlled to transmit as the compulsory intra-frame

mode. Hereafterthe data control method at the time of the fast reproduction of the opposite direction of above-mentioned this example 3 is especially explained using drawing 22drawing 25drawing 26and drawing 27 focusing on operation of the 4th memory 29the still picture packet generating circuit 30and the header attachment **** circuit 34.

[0170]Drawing 26 is a figure for explaining the state of the regenerative data at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this invention. Drawing 27 is a figure showing the partial refreshment on the screen at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this invention. When fast reproduction of an opposite direction is performed to drawing 26 (a)the data for special reproduction reproduced from the rotary head 20 is shown (reproduced intermittently in practice.). The output transport packet outputted to the figure (b) from the switch 32 is shown. The transport packet for one frame is shown in one frame described into the figure. The switching signal of the switch 31 is shown in the figure (c). The data inter-frame [each] outputted to drawing 27 from a digital video tape recorder is shown. The data for special reproduction in which the data of the portion which gave the slash is transmitted by a compulsory intra mode is shown among a figureand other portions show the transmission parts of the still picture packet outputted from the still picture packet generating circuit 30. Also in the fast reproduction of an opposite directionlike the case of a forward directionas shown in drawing 26the picture for special reproduction of one frame is divided into n slice blocksand is transmitted.

[0171]Hereafteroperation of a reversion system is explained. Since the operation to the 3rd error correction decoding circuit 28 is the same as that of Example 2 as mentioned aboveexplanation is omitted. The data for which regenerative-signal processing was performed as mentioned aboveand 3rd 28Cerror correction decoding circuit 4 decoding was given is memorized by the 4th memory 29. A slice is separated from the inputted data for special reproductionthe code amount of the data for special reproduction is counted per sliceand a slice block consists of the 4th memory 29. In the 4th memory 29a slice block consists of places where the code amount of the memorized data for special reproduction became a predetermined valueand data is read from the 4th memory 29.

[0172]After the composition of the data of the above-mentioned 1 slice block is completedthe 4th memory 29 outputs a data output requirement signalthe head included in the above-mentioned slice blockand the macro block address of the last macro block to the still picture packet generating circuit 30. (In additionthe data for special reproduction adds the header information which puts and shows that it is inter-frame (field) to a head like the case of the fast reproduction of the above-mentioned forward direction about the data of the frame for which it does not come to a head.) If the above-mentioned signal is received in the still picture packet generating circuit 30It begins firstand the still picture packet to the macro block in front of [of a top macro block] one is generated and outputted. Under

the present circumstancesthe switch 31 chooses the output of the still picture packet generating circuit 30. And after the output of the still picture packet to the macro block address of the above-mentioned head is completedthe still picture packet generating circuit 30 outputs a data read-out start signal to the 4th memory 29.

[0173]In the 4th memory 29if the above-mentioned signal is receivedthe slice block which generated the point will be read from a head. Under the present circumstancesthe switch 31 chooses the output of the 4th memory 29. An end of read-out of the above-mentioned slice block will output the control signal which shows that read-out of data was completed to the still picture packet generating circuit 30. In the still picture packet generating circuit 30if the above-mentioned signal is receivedthe still picture packet to the last macro block of one frame will be generated and outputted from the next macro block of the last macro block of a slice block. In that casethe switch 31 chooses the output of the still picture packet generating circuit 30 again. If generation of the still picture packet to the last macro block of one frame is completedthe still picture packet generating circuit 30 shall output a no-data packet until the following composition of a slice block is completed.

[0174]On the other handthe output of the switch 31 is inputted into the header attachment **** circuit 34. In this example 3a transport packet is transmitted as INTAFUREMUMODO (mode of between the fields or inter frame prediction) like Example 2. In this casethe data for special reproduction of the slice unit intermittently reproduced at the time of fast reproduction is controlled to transmit as the compulsory intra-frame mode. In the header attachment **** circuit 34. While attaching to the header which detects the header part indicating the transmission mode of the picture in a packet header (MPEG 2 picture header) about the data packet for special reproduction like Example 2and points to inter-frame (or INTAFIRUDO) one and changingThe header unit indicating the decoding mode of a macro block is detectedand this header is attached to the header of the Intra frame modeand is changed. The data packet for special reproduction for which the header was changed is supplied to the output terminal 33 via the switch 32. while the transport packet which transmits the data for special reproduction is transmitted as an inter-frame packet by this -- the data of each macro block -- compulsion -- intra -- it is decoded by an ATV decoder as that of a frame mode.

[0175]On the other handthe still picture packet outputted from the still picture packet generating circuit 30 is supplied to the switch 32 via the header attachment **** circuit 34. It shall generate all over the still picture packet generating circuit 30and a header shall attach the header part of a still picture packet like [in this example 3] Example 2 in the header attachment **** circuit 34and it shall not perform ****.

[0176]The timing chart in the case of dividing drawing 26 into the transport packet of the n frame at the time of the fast reproduction of an opposite directiondividing the data packet for special reproduction of one frame into drawing 27and transmitting and the situation of refreshment of the screen of frame data

transmitted were shown. By transmitting dataas shown in the figurethe screen of one frame will be updated by plural slices for every frameand all the special reproduction pictures will be updated with the n frame (partial refreshment).
[0177]As mentioned abovein this example 3the transport packet to output is transmitted as a packet of INTAFUREMUMODO at the time of the fast reproduction of an opposite direction. In order to freeze a screen by the ATV decoder side at the time of special reproduction (stillness)The slice to which the data packet for special reproduction in one frame is not transmitted can output a good fast reproduction picture like Example 1without being conscious of special reproduction mode by (refer to drawing 26) and an ATV decoder by generating a still picture packet in the still picture packet generating circuit 30.
[0178]At the time of fast reproductionmemory space is reducible as mentioned above by making the memory for fast reproduction memorize by 1 slice block unit rather than making the memory for fast reproduction memorize regenerative data per frameas shown in Example 1. Since a slice is reproduced in an order opposite to the time of record at the time of the fast reproduction of an opposite directionIn order to constitute a reproduced image from an ATV decoderneeded to prepare for the reversion system the memory for ****** which can memorize the data for fast reproduction for at least one frameand needed to put in order and change the reproduced databut. the data of the slice unit reproduced by changing the mode to INTAFUREMUMODO as mentioned above at the time of fast reproduction -- compulsion -- intra -- the above-mentioned memory for ****** becomes unnecessary by changing the mode to a frame mode. In order to make the memory for fast reproduction memorize regenerative data per 1 slice like the time of the fast reproduction of a forward directionit becomes reducible [memory space]. (When dividing data of one frame into ten slice blocks and transmitting it although based also on the size of a slice blockand the refresh period of the data for special reproduction for examplememory space can be reduced to about about 1 / 10.)
[0179]In this example 3since an output transport packet is controlled as mentioned abovethe memory space of the 4th memory 29 is substantially reducible compared with the case of Example 1. As shown in Example 1 that what is necessary is just to arrange the memory which can specifically memorize the data for one slice (it is a part for a number slice depending on the composition of a slice)it is not necessary to arrange the memory for one frame to the reversion system side. In particularin a reproduction special-purpose machinesince it is not necessary to have a memory for one framereduction of circuit structure can be performed. A transport packet can be decoded without carrying out special reproduction mode consciousness about an ATV decoder.
[0180]Example 4. this example 4 describes the constitution method of a still picture packet. MPEG 2 defines the macro block skip only about transmission of an inter-frame packet. It is to fly and transmit if a macro block skip is a macro block in the same slice. (Howeverit cannot skip about the head of a sliceand the last macro block.) If a slice is constituted from a macro block in the same level

macro block as mentioned abovea size will not be asked again. Thereforein this example 4a still picture packet is transmitted using this skip. Drawing 28 is a figure showing the composition of the still picture packet of the slice unit which is one example of this invention. As shown in a figurethe inside of a slice comprises two macro blocks********** comprises 0 andas for the data in each macro blockthe prediction error comprises data of 0. Drawing 28 showed the case where all the same horizontal macro blocks were still picture packets. What is necessary is just to change the macro block address in a macro blockwhen it constitutes a still picture packet from a macro block in the middle of a screen. What is necessary is just to specifically change the relative address of a back macro block. Since the generating day large quantity of a still picture packet can also be lessened while the circuit structure of the circuit which memorizes a still picture packet is reducible if a still picture packet is constituted as mentioned aboveit is effective in circuit control becoming very easy.

[0181]It is not what is restricted to this although the motion vector transmitted the still picture packet and 0 and a prediction error transmitted the packet of 0 in example 5. and above-mentioned Examples 12and 3For examplewhen data is not transmitted at the time of special reproductionthe same effect will be done so if it is a packet which is interpolated by the picture of a previous frame (or previous field). If it constitutes so that the special reproduction picture of one frame may be divided into two or more frames and may be transmitted as used especially in Example 3it cannot be overemphasized that the memory space in a reversion system can be reduced and reduction of circuit structure can be aimed at.

[0182]It is not a thing which is example 6. and which is restricted to this although it said that a still picture packet is generated per transport packet in the above-mentioned exampleFor exampleit is not what the case so that it may constitute per transport packet was described when a slice block was constituted in Example 2 or 3but is restricted to thisThe same effect is done soeven if 0 and a prediction error insert the macro block of 0 and the above-mentioned motion vector generates a transport packet from the middle of the reproduced transport packet. The same effect is done soeven if the data for special reproduction (slice unit) reproduced following the macro block which shows the above-mentioned still picture is inserted and it constitutes a transport packet.

[0183]The same effect will be done soif the transport packet which is example 7. and which does not restrict to this although the data for special reproduction has been treated as data of a frame image in this exampleand has been transmitted is a field imageit will treat as a field image and same processing will be performed. It is not what is restricted to this although the case where the above-mentioned example showed to drawing 11 as a recording format of data was explainedIn the digital video tape recorder which records the digital signal to which high efficiency coding was given by the low bit rate coding method using the motion compensation prediction represented by MPEG 2The data in which intra coding was performed as data for special reproduction is separated from the above-mentioned digital signalIf it is digital signal playback equipment which has the format to which the

data for special reproduction separated [above-mentioned] is recorded on the area on a recording medium appointed beforehandit cannot be overemphasized that the same effect is done so by the above-mentioned control. In the above-mentioned examplealthough a digital video tape recorder is described as one example of digital signal playback equipmentit does not restrict to thisand even if it uses for the control at the time of special reproductionsuch as a disk player which records the above-mentioned signal in an above-mentioned waythe same effect is done so.

[0184]

[Effect of the Invention]It comprises this inventionas explained above. Thereforean effect as taken below is done so.

[0185]the inside of the frame or the field which was inputted in the state of the packet according to the digital signal playback equipment of this invention according to claim 1 -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium currently recorded on the positionThe data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand a still picture slice data generating means in which all the macro blocks in a slice generate the slice data whose prediction error a motion vector is 0 in 0Since it constitutes so that predetermined may carry out the frame number partial output of the output of the above-mentioned still picture slice generating meansand the above-mentioned still picture slice generating means may be controlled after outputting one frame separated from said data storage meansor the above-mentioned data for special reproduction for the 1 fieldWhile being able to reduce memory space and being able to aim at reduction of circuit structureit has the effect that special reproduction can be realized without making an ATV decoder conscious of special reproduction mode.

[0186]the inside of the frame or the field which was inputted in the state of the packet according to the digital signal playback equipment of this invention according to claim 2 -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium

currently recorded on the positionThe data separation means which separates the above-mentioned data for special reproduction from a regenerative signal at the time of special reproductionIt has a data storage means which memorizes the separated above-mentioned data for special reproductionand a still picture slice data generating means in which all the macro blocks in a slice generate the slice data whose prediction error a motion vector is 0 in 0The above-mentioned data for special reproduction separated from the regenerative data reproduced intermittently by the above-mentioned data separation means 1 or plural slicesand the transport packet for one **** for an output of a still picture slice data generating means -- while carrying out -- the above-mentioned transport packet -- the field. Or since a packet is constituted so that the data for special reproduction which considered it as the packet in inter-frame-prediction modeand was reproduced by the above-mentioned intermittent target may be made into the compulsory intra-frame mode and may be transmittedIt has the effect that the memory space at the time of fast reproduction can be reducedand circuit structure can be reduced.

[0187]According to the digital signal playback equipment of this invention according to claim 3at the time of still playback. Since the output in the above-mentioned still picture packet creating means is constituted after the end of a final data output of the above-mentioned frame or frame reproduced at the time of ordinary reproduction so that it may always outputIt is not necessary to provide the memory which stores the Intra information for one frame in the digital video tape recorder side also in the still playback which does not use the data for special reproductionand has an effect which can constitute a good reproduced image by using the still picture packet creating means used at the time of fast reproduction.

[0188]According to the digital signal playback equipment of this invention according to claim 4at the time after the mode to fast reproduction. Until a servo system locks and the intra-frame data for [above-mentioned] special reproduction is reproduced from the above-mentioned fast reproduction areaSince it constitutes so that the output of the above-mentioned still picture packet creating means may be chosenand the above-mentioned data switching means may be controlledit has the effect that the mode or subsequent ones can be performed smoothly without disturbing a reproduced image at the time of mode transition.

[0189]Since according to the digital signal playback equipment of this invention according to claim 5 it constitutes so that the above-mentioned control system may be used at least at the time of the special reproduction of an opposite directionthe data provided in reverse direction reproduction arrangingand changingwhile the memory space at the time of fast reproduction is reducible -- business -- a memory becomes unnecessary and it has the effect that the further circuit structure is reducible.

[0190]the inside of the frame or the field which was inputted in the state of the packet according to the digital signal playback equipment of this invention

according to claim 6 -- orWhile transparent record of a frame or the digital video signal by which interfield coding was carried outand the digital audio signals is carried outThe data for special reproduction used at the time of special reproduction from the above-mentioned digital video signal with which a frame or field inner code-ization was performed from the above-mentioned bit stream is generatedIn the digital signal playback equipment in which the data for special reproduction generated [above-mentioned] reproduces the recording medium currently recorded on the positionWhen the data separation means which separates the above-mentioned data for special reproduction from a regenerative signaland the data outputted from the digital signal recording and reproducing device are decoded and reproduced image data is restoredWhen it has a specific area fixed packet creating means which generates the packet for standing the signal of the specific area on a screen still and a reproduced image is constituted using the data reproduced intermittently at the time of special reproductionthe output of the above-mentioned specific packet fixing meansSince it constitutes so that the above-mentioned regenerative data is switchedand the above-mentioned data for special reproduction of one frame may be divided into a multiple frame and may be transmittedIt has the effect that the memory space at the time of fast reproduction is reducible.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a block lineblock diagram of the reversion system of the digital video tape recorder which is one example of this invention.

[Drawing 2]It is a block lineblock diagram of the 3rd error correction decoding circuit 28 that is one example of this invention.

[Drawing 3]It is a block lineblock diagram of the error correction circuit 43 which is one example of this invention.

[Drawing 4]It is a figure showing arrangement of the data in 1 track which is one example of this invention based on SD standard.

[Drawing 5]They are the rotary head 20 on the typical rotating drum 19 used at the time of an SD mode (a)and a plot plan of 20 (b).

[Drawing 6]It is a figure showing the data packet which is one example of this inventionand the transport packet figure where (a) is contained in an input bit streamand (b) are recording data packet figures recorded on magnetic tape.

[Drawing 7]It is a code configuration figure of the error correcting code added to the data for special reproduction of the digital video tape recorder which is one example of this invention.

[Drawing 8]It is a figure showing the number of sink blocks in which the data acquisition at the time of fast reproduction is possible.

[Drawing 9]They are a plot plan of the data recording area for special reproduction in the track of the digital video tape recorder which is one example of this

inventionand a figure showing arrangement of the data recorded on the data recording area for special reproduction.
[Drawing 10]It is a figure showing the split method of 1 error correction block of the 16X (−14 X) data of the digital video tape recorder which is one example of this invention.
[Drawing 11]It is a figure showing the track format of the digital video tape recorder which is one example of this invention.
[Drawing 12]It is a head scanning-locus figure of the rotary head 20 (a) when the digital video tape recorder which is one example of this invention performs twice4 times8 timesand 16X fast reproduction.
[Drawing 13]It is an explanatory view of operation for explaining the tracking control operation of the digital video tape recorder which is one example of this invention.
[Drawing 14]It is a figure explaining general C1 decoding algorithm used for a digital video tape recorder.
[Drawing 15]It is a figure explaining general C4 decoding algorithm used for a digital video tape recorder.
[Drawing 16]It is a figure explaining the addition algorithm of the data update flag of the digital video tape recorder which is one example of this invention.
[Drawing 17]It is a figure explaining C4 decoding algorithm of the digital video tape recorder which is one example of this invention.
[Drawing 18]It is an explanatory view of operation for explaining C4 decoding algorithm of the digital video tape recorder which is one example of this invention.
[Drawing 19]It is a timing chart of the special reproduction of the digital video tape recorder which is one example of this invention.
[Drawing 20]It is a timing chart at the time of shifting to special reproduction from the ordinary reproduction of the digital video tape recorder which is one example of this invention.
[Drawing 21]It is an explanatory view of operation showing the output form of the data for one frame at the time of the special reproduction of the digital video tape recorder which is one example of this invention.
[Drawing 22]It is a block lineblock diagram of the reversion system of the digital video tape recorder which is one example of this invention.
[Drawing 23]It is a figure for explaining the state of the regenerative data at the time of the special reproduction for Masakata of the digital video tape recorder which is one example of this invention.
[Drawing 24]It is a figure showing the partial refreshment on the screen at the time of the special reproduction for Masakata of the digital video tape recorder which is one example of this invention.
[Drawing 25]It is an explanatory view of operation at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this invention.
[Drawing 26]It is a figure for explaining the state of the regenerative data at the time of the special reproduction of the opposite direction of the digital video tape

recorder which is one example of this invention.
[Drawing 27]It is a figure showing the partial refreshment on the screen at the time of the special reproduction of the opposite direction of the digital video tape recorder which is one example of this invention.
[Drawing 28]It is a figure showing the example of composition of the still picture packet at the time of using a macro block skip within the slice which is one example of this invention.
[Drawing 29]It is a track pattern figure of a common home digital video tape recorder.
[Drawing 30]It is a figure showing the head scanning locus of the rotary head at the time of the ordinary reproduction of the conventional digital video tape recorderand fast reproduction.
[Drawing 31]It is a block lineblock diagram of the conventional bit stream recorder in which fast reproduction is possible.
[Drawing 32]It is a figure showing the outline at the time of the ordinary reproduction of the conventional digital video tape recorderand fast reproduction.
[Drawing 33]It is a head scanning-locus figure at the time of general fast reproduction.
[Drawing 34]It is a figure explaining the area of the overlap at the time of two or more conventional fast reproduction speed.
[Drawing 35]It is a head scanning-locus figure (5X and 9X) in the conventional digital video tape recorder.
[Drawing 36]They are two head scanning-locus figures at the time of the 5X reproduction in the conventional digital video tape recorder.
[Drawing 37]It is a track arrangement figure in the conventional digital video tape recorder.
[Drawing 38]It is a data format figure of the video-signal recording area in 1 track of the video signal in SD standard.
[Drawing 39]It is a figure showing the composition of one sink block in SD standard.
[Description of Notations]
27 The 3rd memory and 29 [Header attachment **** circuit.] A still picture packet generating circuitand 31 and 32 The 4th memory and 30 A switch and 34